

74HC03; 74HCT03

Quad 2-input NAND gate; open-drain output

Rev. 4 — 27 November 2015

Product data sheet

1. General description

The 74HC03; 74HCT03 is a quad 2-input NAND gate with open-drain outputs. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Input levels:
 - ◆ For 74HC03: CMOS level
 - ◆ For 74HCT03: TTL level
- Complies with JEDEC standard no. 7A
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

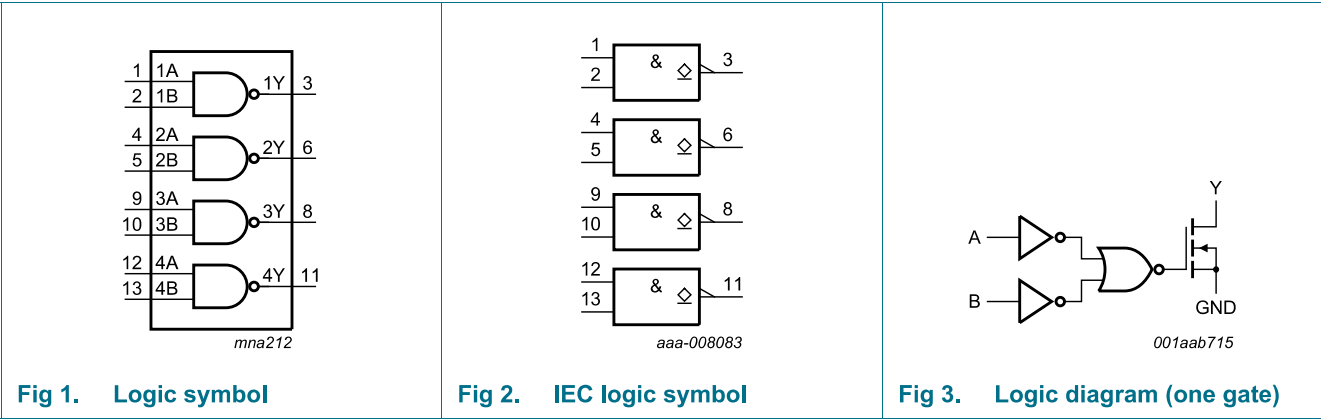
3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC03D	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT03D				
74HC03DB	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HCT03DB				
74HC03PW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT03PW				

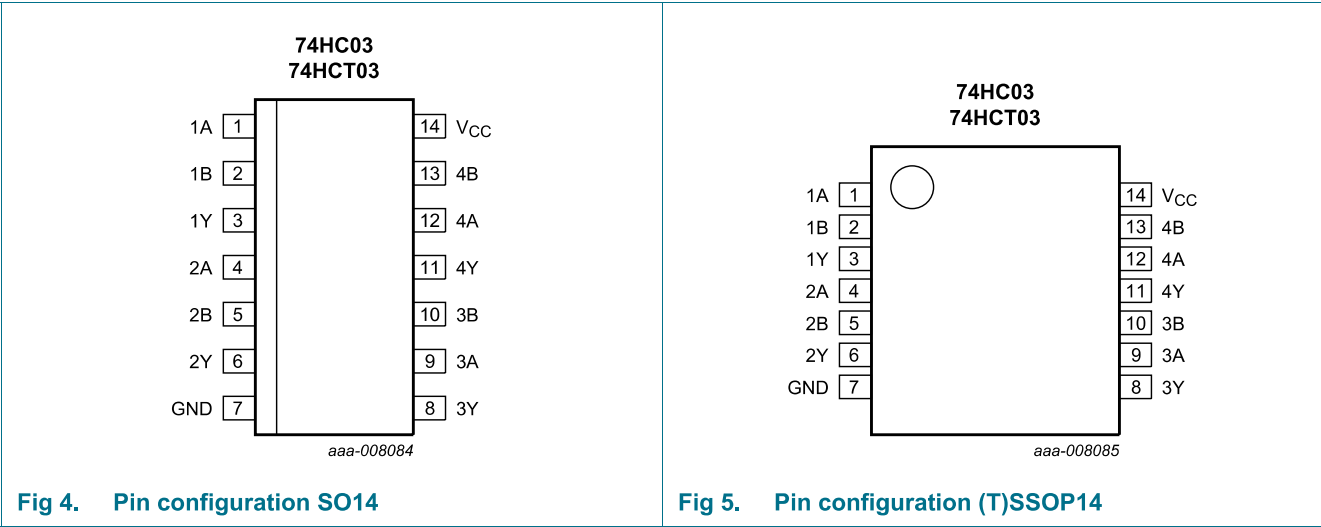


4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 4A	1, 4, 9, 12	data input
1B to 4B	2, 5, 10, 13	data input
1Y to 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table^[1]

Input		Output
nA	nB	nY
L	L	Z
L	H	Z
H	L	Z
H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		−0.5	+7	V
V _O	output voltage	^[1]	−0.5	+7	V
I _{IK}	input clamping current	V _I < −0.5 V or V _I > V _{CC} + 0.5 V ^[1]	-	±20	mA
I _{OK}	output clamping current	V _O < −0.5 V ^[1]	-	−20	mA
I _O	output current	−0.5 V < V _O	-	−25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		−50	-	mA
T _{stg}	storage temperature		−65	+150	°C
P _{tot}	total power dissipation	^[2]			
	SO14 and (T)SSOP14 packages		-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For (T)SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC03			74HCT03			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		−40	+25	+125	−40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC03										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	0.1	-	-	±1	-	±1	μA
I _{OZ}	OFF-state output current	per input pin; V _I = V _{IL} ; V _O = V _{CC} or GND; other inputs at V _{CC} or GND; V _{CC} = 6.0 V; I _O = 0 A	-	-	±0.5	-	±5.0	-	±10	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	2.0	-	-	20	-	40	μA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT03										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1	-	±1	μA
I _{OZ}	OFF-state output current	per input pin; V _I = V _{IL} ; V _O = V _{CC} or GND; other inputs at V _{CC} or GND; V _{CC} = 5.5 V; I _O = 0 A	-	-	±0.5	-	±5.0	-	±10	μA

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	2.0	-	20	-	40	μ A
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1$ V; $I_O = 0$ A; other inputs at V_{CC} or GND; $V_{CC} = 4.5$ V to 5.5 V	-	100	360	-	450	-	490	μ A
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristicsGND = 0 V; $C_L = 50$ pF; for test circuit, see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +125 °C		Unit
			Min	Typ	Max	Max (85 °C)	Max (125 °C)	
74HC03								
t _{pd}	propagation delay	nA, nB to nY; see Figure 6 [1]						
		V _{CC} = 2.0 V	-	28	95	120	145	ns
		V _{CC} = 4.5 V	-	10	19	24	29	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	8	-	-	-	ns
		V _{CC} = 6.0 V	-	8	16	20	25	ns
t _t	transition time	see Figure 6 [2]						
		V _{CC} = 2.0 V	-	19	75	95	110	ns
		V _{CC} = 4.5 V	-	7	15	19	22	ns
		V _{CC} = 6.0 V	-	6	13	16	19	ns
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} [3]	-	4	-	-	-	pF

Table 7. Dynamic characteristics ...continued
GND = 0 V; C_L = 50 pF; for test circuit, see Figure 7.

Symbol	Parameter	Conditions	25 °C			−40 °C to +125 °C		Unit
			Min	Typ	Max	Max (85 °C)	Max (125 °C)	
74HCT03								
t _{pd}	propagation delay	nA, nB to nY; see Figure 6 [1]						
		V _{CC} = 4.5 V	-	12	24	30	36	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	10	-	-	-	ns
t _t	transition time	V _{CC} = 4.5 V; see Figure 6 [2]	-	7	15	19	22	ns
C _{PD}	power dissipation capacitance	per package; [3] V _I = GND to V _{CC} − 1.5 V	-	4	-	-	-	pF

- [1] t_{pd} is the same as t_{PLZ} and t_{PZL}.
- [2] t_t is the same as t_{THL}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms

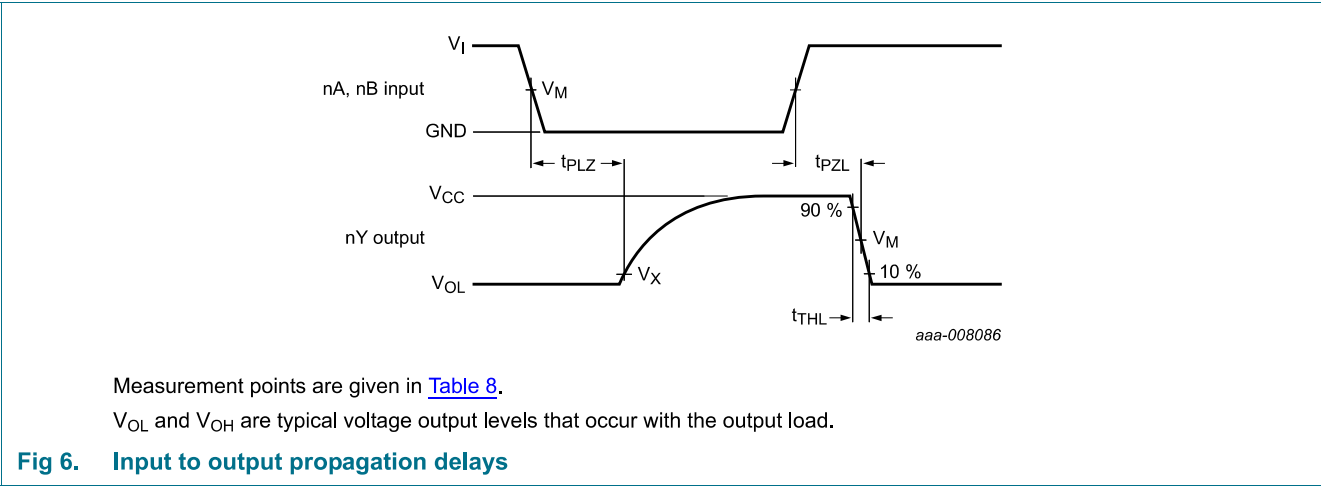


Table 8. Measurement points

Type	Input	Output	
	V _M	V _M	V _X
74HC03	0.5V _{CC}	0.5V _{CC}	0.1V _{CC}
74HCT03	1.3 V	1.3 V	0.1V _{CC}

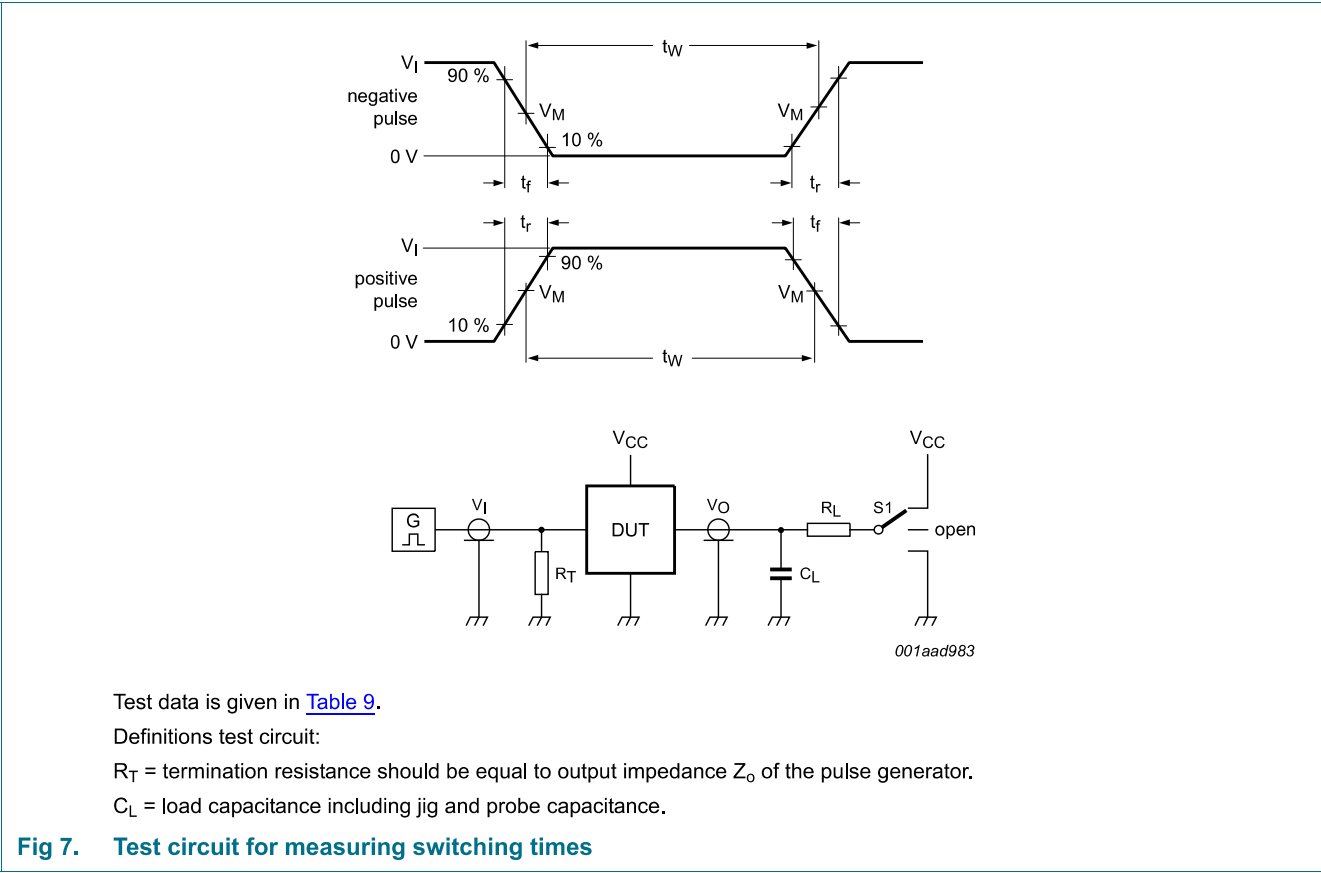


Table 9. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	
74HC03	V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	V_{CC}
74HCT03	3.0 V	6 ns	15 pF, 50 pF	1 k Ω	V_{CC}

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

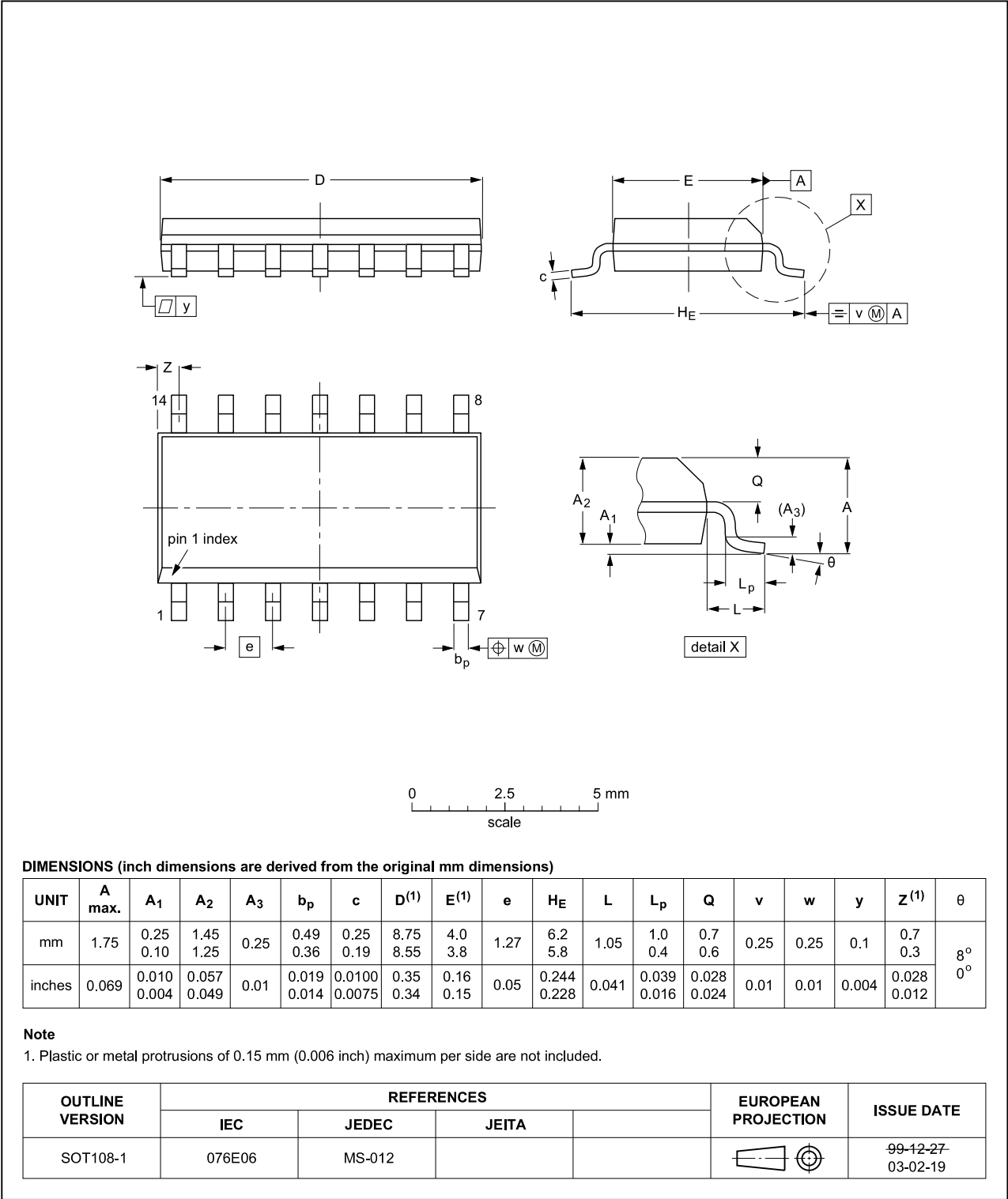


Fig 8. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

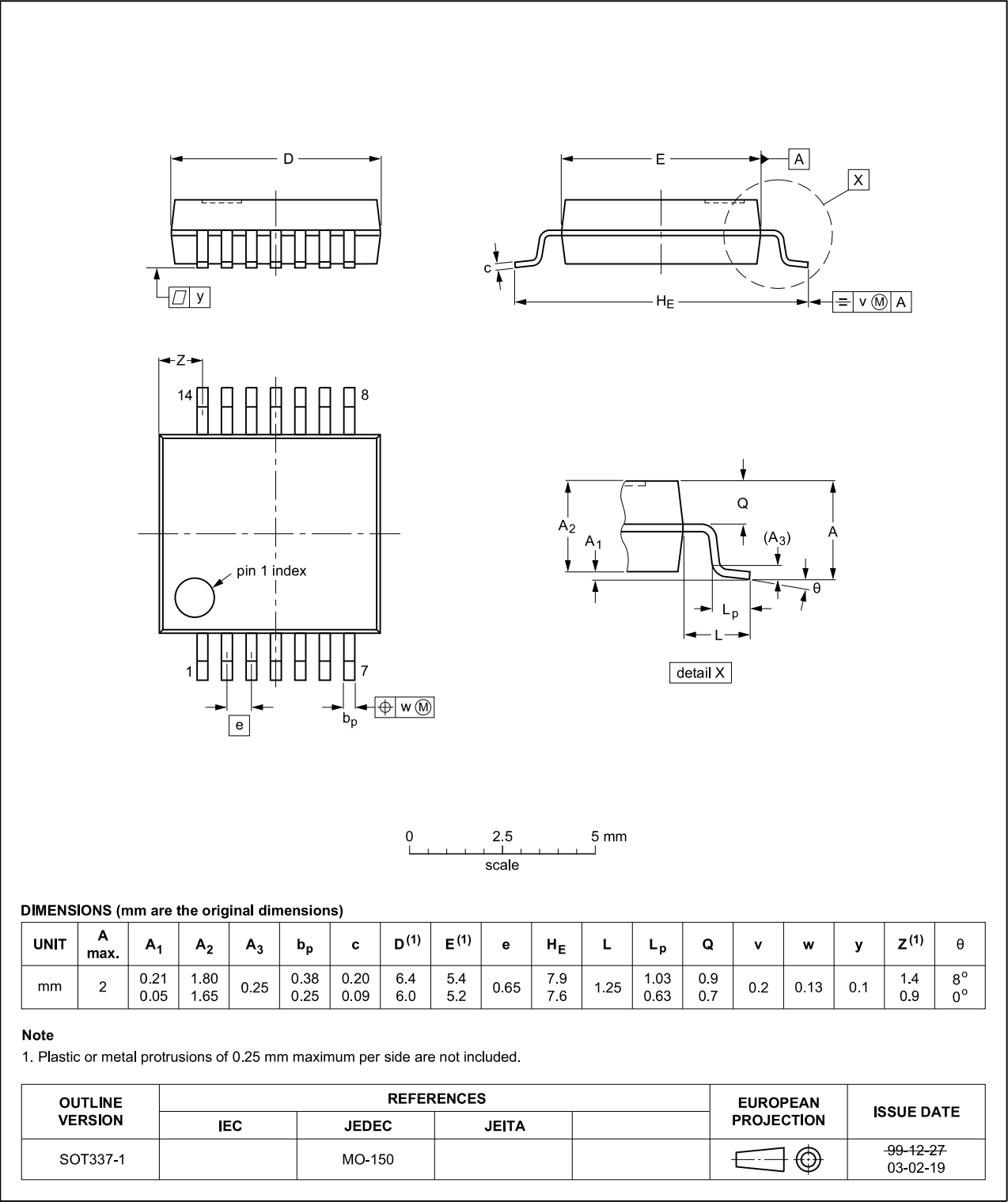
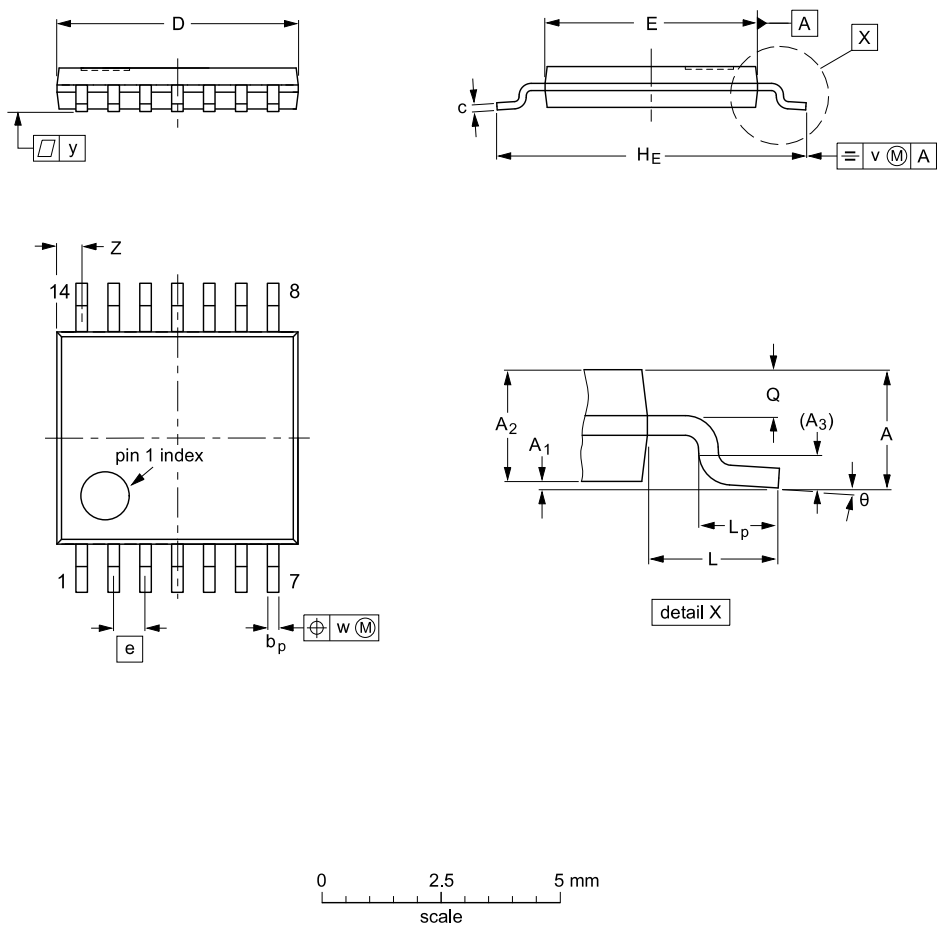


Fig 9. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

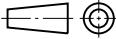
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				-99-12-27- 03-02-18

Fig 10. Package outline SOT402-1 (TSSOP14)