

74HC163; 74HCT163

Presettable synchronous 4-bit binary counter; synchronous reset

Rev. 4 — 28 December 2015

Product data sheet

1. General description

The 74HC163; 74HCT163 is a synchronous presettable binary counter with an internal look-ahead carry. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP). The outputs (Q0 to Q3) of the counters may be preset to a HIGH or LOW. A LOW at the parallel enable input ($\overline{PE}$) disables the counting action. It causes the data at the data inputs (D0 to D3) to be loaded into the counter on the positive-going edge of the clock. Preset takes place regardless of the levels at count enable inputs (CEP and CET). A LOW at the master reset input ($\overline{MR}$) sets Q0 to Q3 LOW after the next positive-going transition on the clock input (CP). This action occurs regardless of the levels at input pins $\overline{PE}$, CET and CEP. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate. The look-ahead carry simplifies serial cascading of the counters. Both CEP and CET must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH output of Q0. This pulse can be used to enable the next cascaded stage. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

The CP to TC propagation delay and CEP to CP set-up time determine the maximum clock frequency for the cascaded counters according to the following formula:

$$f_{max} = \frac{1}{t_{P(max)}(CP to TC) + t_{SU}(CEP to CP)}$$

2. Features and benefits

- Complies with JEDEC standard no. 7A
- Input levels:
 - ◆ For 74HC163: CMOS level
 - ◆ For 74HCT163: TTL level
- Synchronous counting and loading
- 2 count enable inputs for n-bit cascading
- Synchronous reset
- Positive-edge triggered clock
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

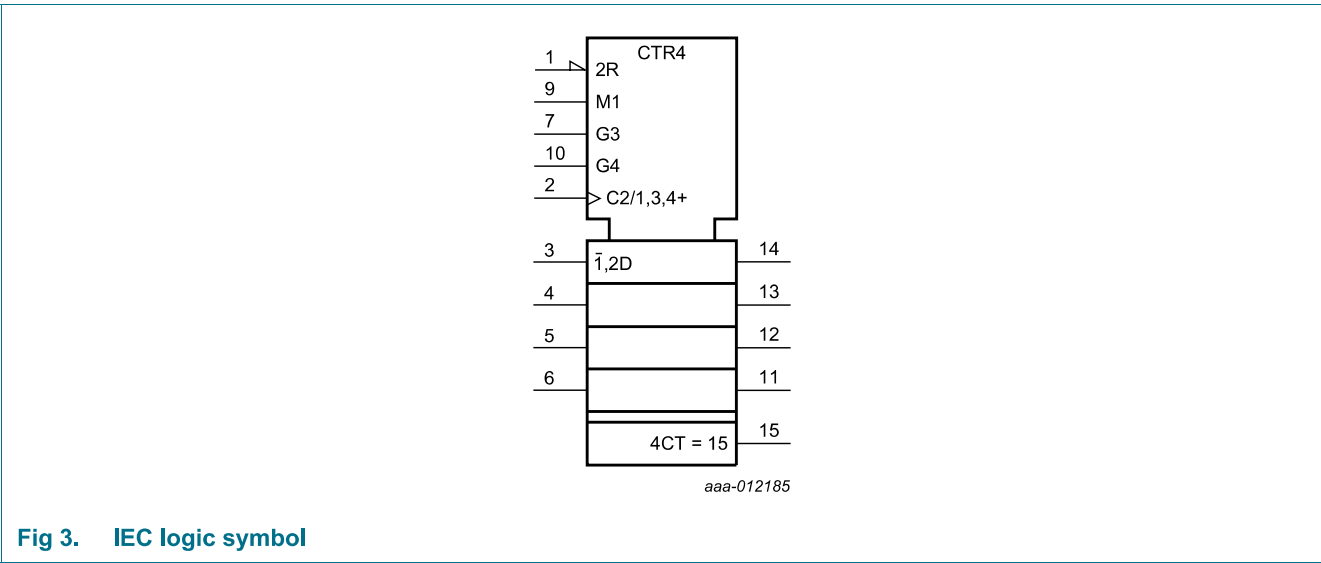
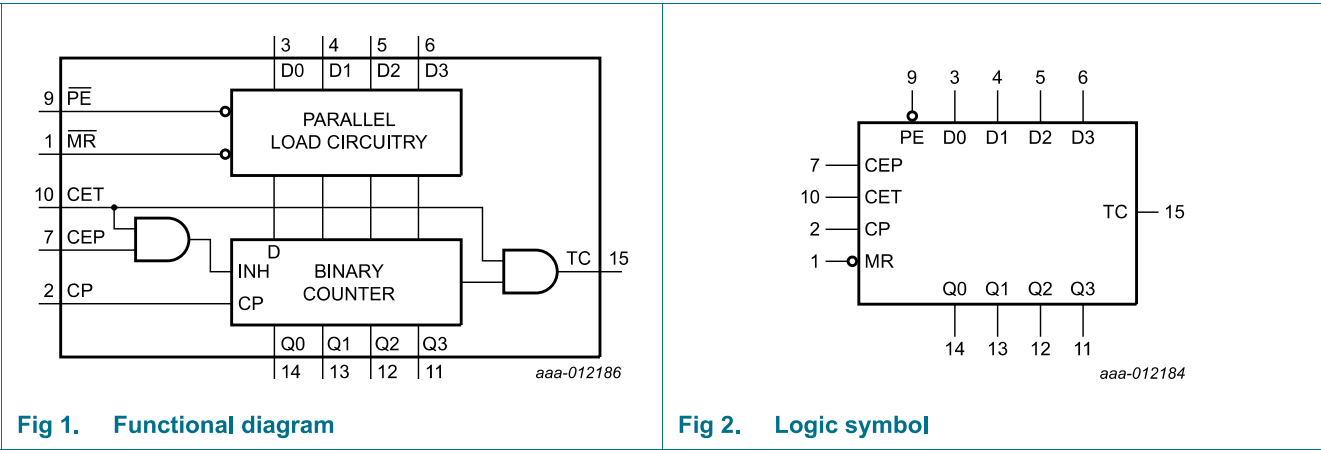


3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC163D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT163D				
74HC163DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT163DB				
74HC163PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT163PW				

4. Functional diagram



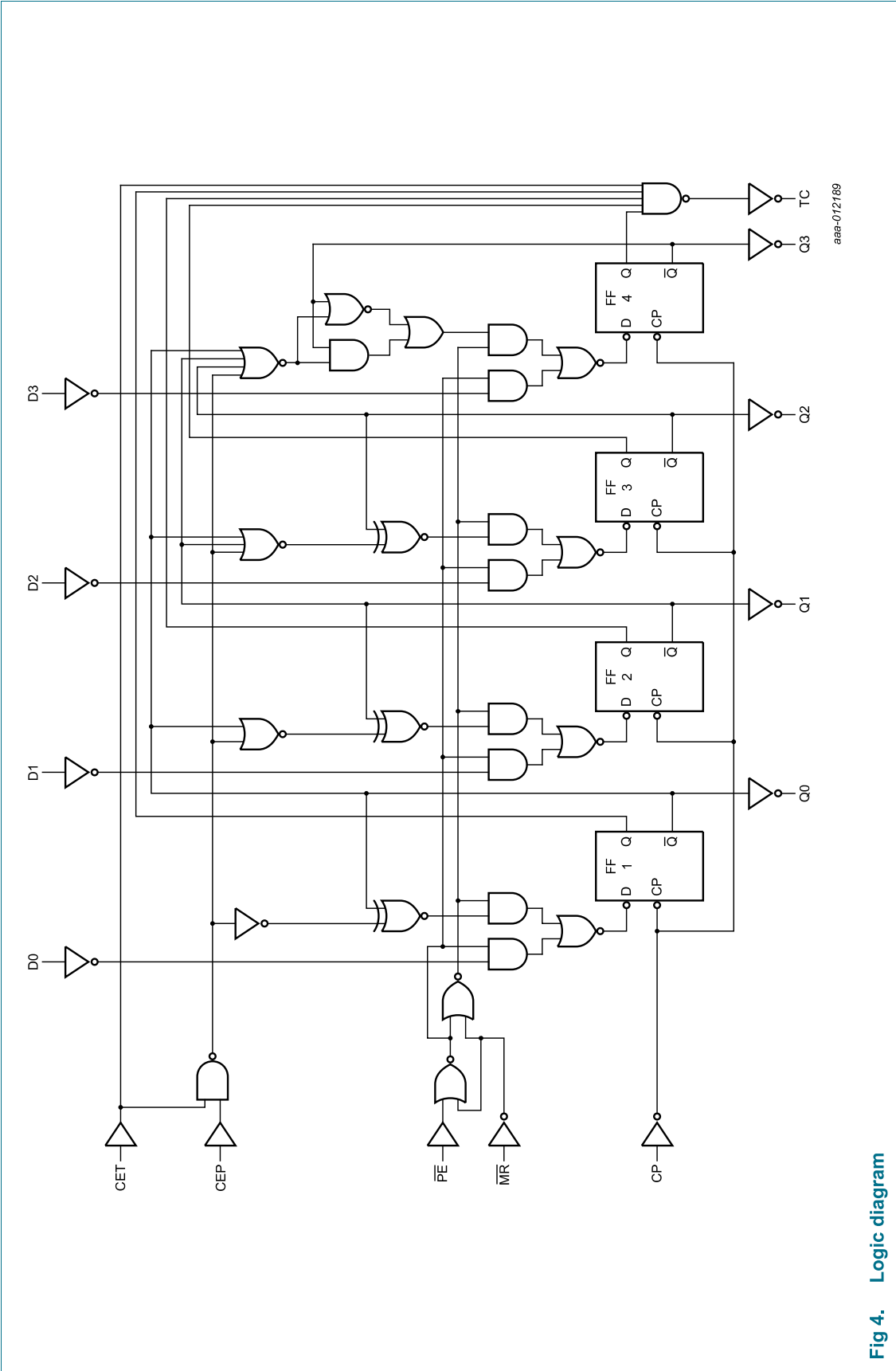


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

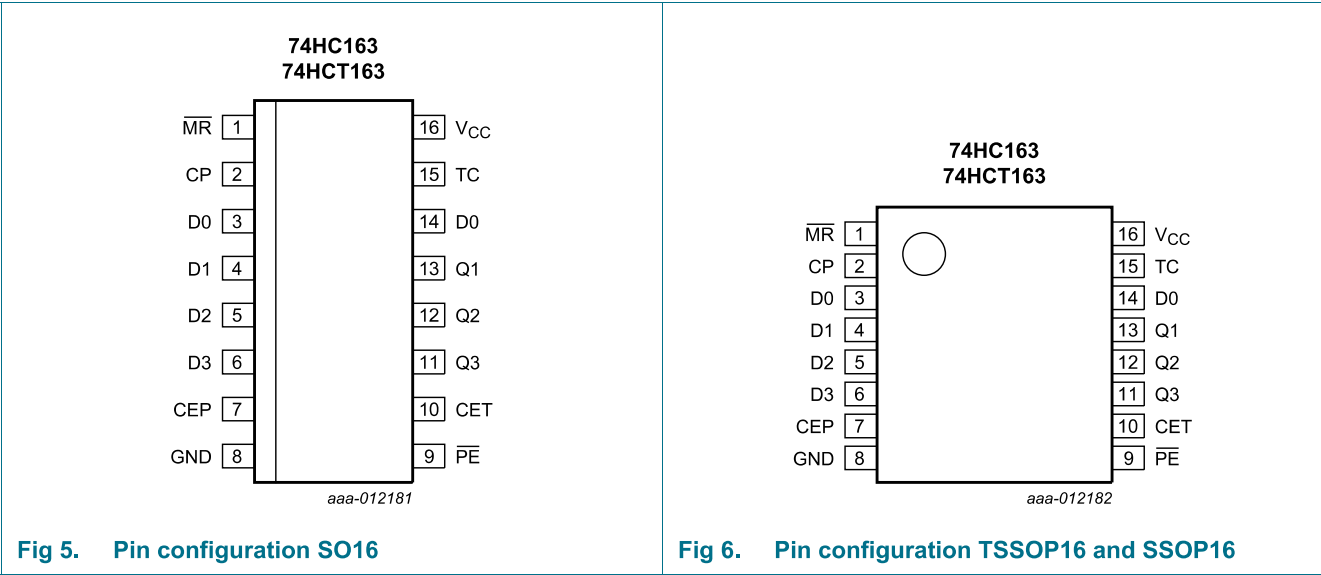


Fig 5. Pin configuration SO16

Fig 6. Pin configuration TSSOP16 and SSOP16

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
MR	1	synchronous master reset (active LOW)
CP	2	clock input (LOW-to-HIGH, edge triggered)
D0, D1, D2, D3	3, 4, 5, 6	data input
CEP	7	count enable input
GND	8	ground (0 V)
PE	9	parallel enable input (active LOW)
CET	10	count enable carry input
Q0, Q1, Q2, Q3	14, 13, 12, 11	flip-flop output
TC	15	terminal count output
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function table^[1]

Operating mode	Inputs						Outputs	
	MR	CP	CEP	CET	PE	Dn	Qn	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	L
Count	h	↑	h	h	h	X	count	
Hold (do nothing)	h	X	l	X	h	X	qn	L
	h	X	X	l	h	X	qn	L

- [1] The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH);
H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition;
X = don't care;
↑ = LOW-to-HIGH clock transition.

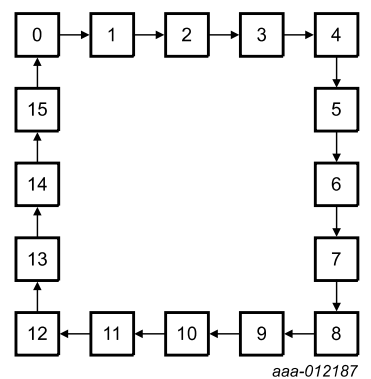
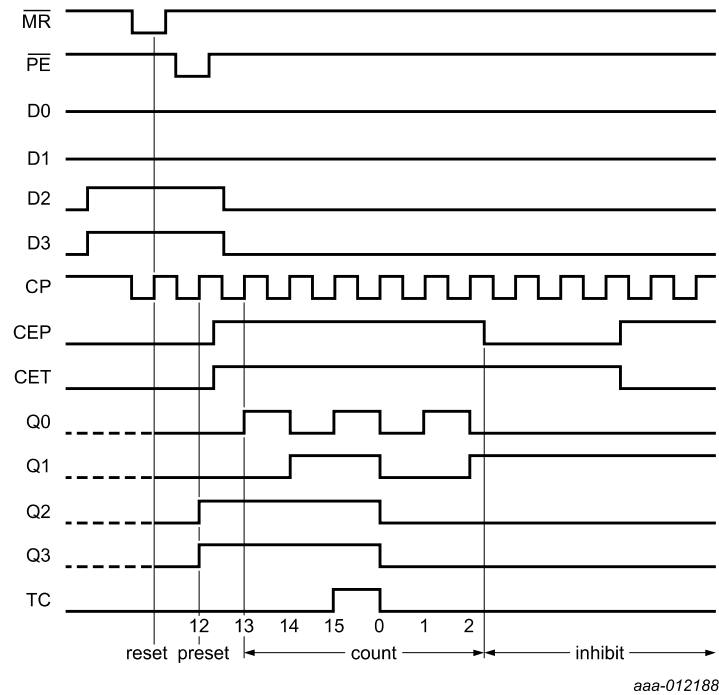


Fig 7. State diagram

**Sequence**

reset outputs to zero; preset to binary 12; count to 13, 14, 15, zero, one and two; inhibit.

Fig 8. Typical timing sequence

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5 \text{ V}$ or $V_O > V_{CC} + 0.5 \text{ V}$	-	± 20	mA
I_O	output current	$V_O = -0.5 \text{ V}$ to $V_{CC} + 0.5 \text{ V}$	-	± 25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	SO16 package [1]	-	500	mW
		(T)SSOP16 package [1]	-	500	mW

[1] For SO16 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.

For (T)SSOP16 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC163			74HCT163			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC163										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = −20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = −20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = −20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = −4.0; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	I _O = −5.2; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
		V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
I _I	input leakage current	I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
		V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80.0	-	160.0	μA

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT163										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = –20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = –4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80.0	-	160.0	µA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} – 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A								
		pin $\overline{\text{MR}}$	-	95	342	-	427.5	-	465.5	µA
		pin CP	-	110	396	-	495	-	539	µA
		pin CEP and Dn	-	25	90	-	112.5	-	122.5	µA
		pin CET	-	75	270	-	337.5	-	367.5	µA
		pin $\overline{\text{PE}}$	-	30	108	-	135	-	147	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 14](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC163										
t _{pd}	propagation delay	CP to Qn; see Figure 9 [1]								
		V _{CC} = 2.0 V	-	55	185	-	230	-	280	ns
		V _{CC} = 4.5 V	-	20	37	-	46	-	56	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	17	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	16	31	-	39	-	48	ns
		CP to TC; see Figure 9								
		V _{CC} = 2.0 V	-	69	215	-	270	-	320	ns
		V _{CC} = 4.5 V	-	25	43	-	54	-	65	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	21	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	20	37	-	46	-	55	ns
		CET to TC; see Figure 10								
		V _{CC} = 2.0 V	-	36	120	-	150	-	180	ns
		V _{CC} = 4.5 V	-	13	24	-	30	-	36	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	11	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	10	20	-	26	-	31	ns
t _t	transition time	see Figure 9 and Figure 10 [2]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t _w	pulse width	CP; HIGH or LOW; see Figure 9								
		V _{CC} = 2.0 V	80	17	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	6	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	5	-	17	-	20	-	ns

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 14](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{su}	set-up time	$\overline{MR}$, Dn to CP; see Figure 11 and Figure 12								
		$V_{CC} = 2.0$ V	80	17	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	6	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	5	-	17	-	20	-	ns
		$\overline{PE}$ to CP; see Figure 11								
		$V_{CC} = 2.0$ V	80	22	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	8	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	6	-	17	-	20	-	ns
		CEP, CET to CP; see Figure 13								
		$V_{CC} = 2.0$ V	175	58	-	220	-	265	-	ns
		$V_{CC} = 4.5$ V	35	21	-	44	-	53	-	ns
		$V_{CC} = 6.0$ V	30	17	-	37	-	45	-	ns
t_h	hold time	Dn, $\overline{PE}$, CEP, CET, $\overline{MR}$ to CP; see Figure 11 , Figure 12 and Figure 13								
		$V_{CC} = 2.0$ V	0	–14	-	0	-	0	-	ns
		$V_{CC} = 4.5$ V	0	–5	-	0	-	0	-	ns
		$V_{CC} = 6.0$ V	0	–4	-	0	-	0	-	ns
f_{max}	maximum frequency	CP; see Figure 9								
		$V_{CC} = 2.0$ V	5	15	-	4	-	4	-	MHz
		$V_{CC} = 4.5$ V	27	46	-	22	-	18	-	MHz
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	51	-	-	-	-	-	MHz
		$V_{CC} = 6.0$ V	32	55	-	26	-	21	-	MHz
C_{PD}	power dissipation capacitance	$V_I = GND$ to V_{CC} ; $V_{CC} = 5$ V; $f_i = 1$ MHz [3]	-	33	-	-	-	-	-	pF

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 14](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT193										
t _{pd}	propagation delay	CP to Qn; see Figure 9 [1]								
		V _{CC} = 4.5 V	-	23	39	-	49	-	59	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	20	-	-	-	-	-	ns
		CP to TC; see Figure 9								
		V _{CC} = 4.5 V	-	29	49	-	61	-	74	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	25	-	-	-	-	-	ns
		CET to TC; see Figure 10								
		V _{CC} = 4.5 V	-	17	32	-	44	-	48	ns
V _{CC} = 5.0 V; C _L = 15 pF	-	14	-	-	-	-	-	ns		
t _t	transition time	see Figure 9 and Figure 10 [2]								
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t _w	pulse width	CP; HIGH or LOW; see Figure 9								
		V _{CC} = 4.5 V	20	6	-	25	-	30	-	ns
t _{su}	set-up time	$\overline{MR}$, Dn to CP; see Figure 11 and Figure 12								
		V _{CC} = 4.5 V	20	9	-	25	-	30	-	ns
		$\overline{PE}$ to CP; see Figure 11								
		V _{CC} = 4.5 V	20	11	-	25	-	30	-	ns
		CEP, CET to CP; see Figure 13								
V _{CC} = 4.5 V	40	24	-	50	-	60	-	ns		
t _h	hold time	Dn, $\overline{PE}$, CEP, CET, $\overline{MR}$ to CP; see Figure 11 , Figure 12 and Figure 13								
		V _{CC} = 4.5 V	0	–5	-	0	-	0	-	ns
f _{max}	maximum frequency	CP; see Figure 9								
		V _{CC} = 4.5 V	26	45	-	21	-	17	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF	-	50	-	-	-	-	-	MHz

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 14](#).

Symbol	Parameter	Conditions		25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } V_{CC} - 1.5 \text{ V};$ $V_{CC} = 5 \text{ V}; f_i = 1 \text{ MHz}$	[3]	-	35	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH} .

[2] t_i is the same as t_{THL} and t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

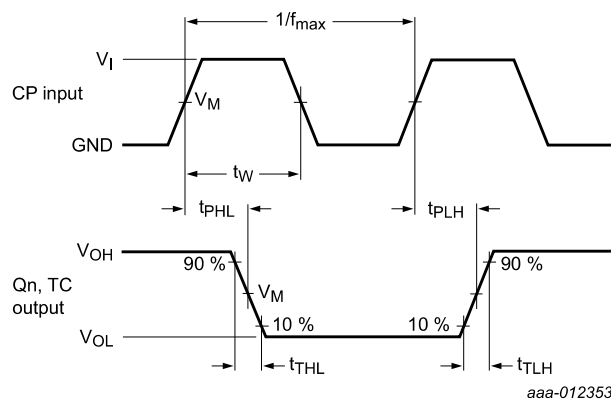
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

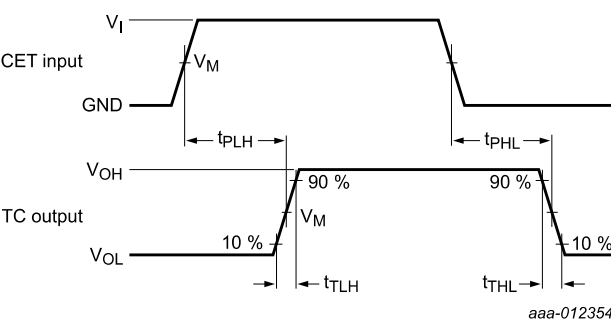
11. Waveforms



Measurement points are given in [Table 8](#).

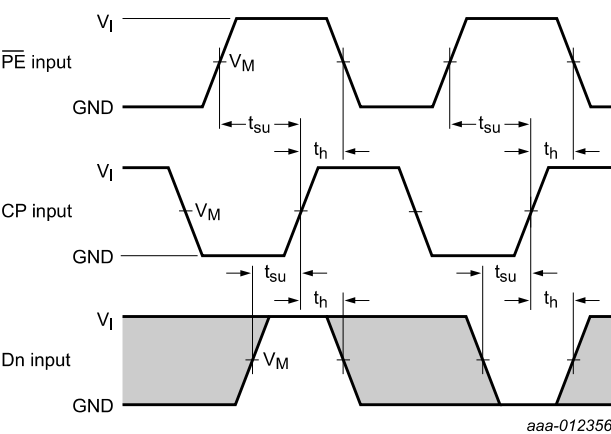
Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 9. The clock (CP) to outputs (Qn, TC) propagation delays, pulse width, output transition times and maximum frequency



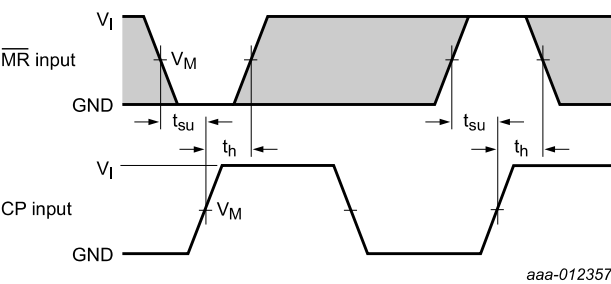
Measurement points are given in [Table 8](#).
 Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 10. The count enable carry input (CET) to terminal count output (TC) propagation delays and output transition times



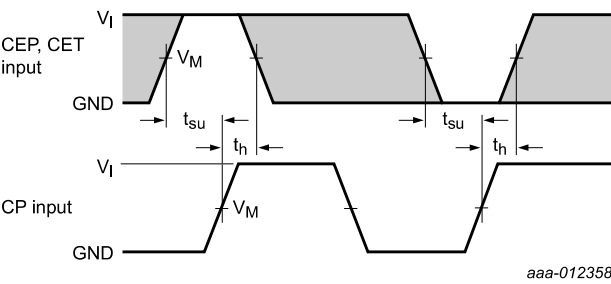
The shaded areas indicate when the input is permitted to change for predictable output performance.
 Measurement points are given in [Table 8](#).

Fig 11. The data input (Dn) and parallel enable input ($\overline{PE}$) set-up and hold times



The shaded areas indicate when the input is permitted to change for predictable output performance. Measurement points are given in [Table 8](#).

Fig 12. The master reset ($\overline{\text{MR}}$) set-up and hold times



The shaded areas indicate when the input is permitted to change for predictable output performance. Measurement points are given in [Table 8](#).

Fig 13. The count enable input (CEP) and count enable carry input (CET) set-up and hold times

Table 8. Measurement points

Type	Input		Output
	V_M	V_I	V_M
74HC163	$0.5 \times V_{CC}$	GND to V_{CC}	$0.5 \times V_{CC}$
74HCT163	1.3 V	GND to 3 V	1.3 V

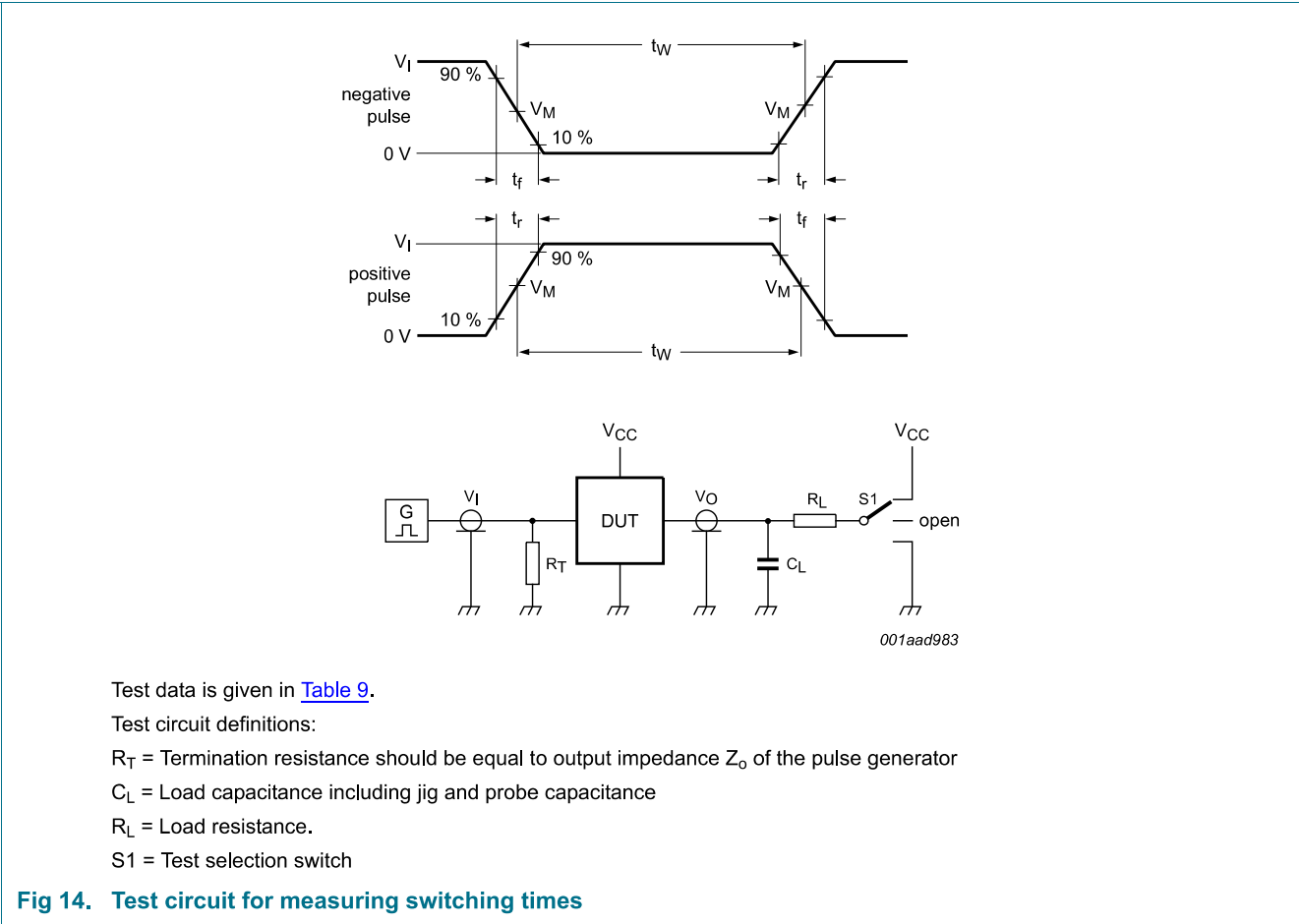


Table 9. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	
74HC163	V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	open
74HCT163	3 V	6 ns	15 pF, 50 pF	1 k Ω	open

12. Application information

The 74HC163; 74HCT163 facilitate designing counters of any modulus with minimal external logic. The output is glitch-free due to the synchronous reset.

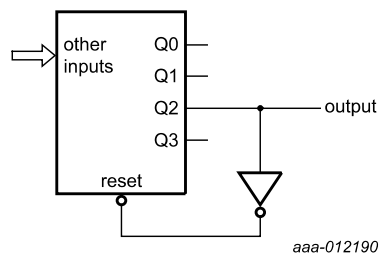


Fig 15. Modulo-5 counter

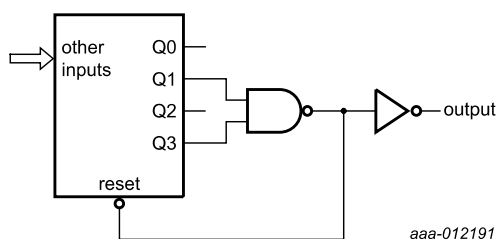


Fig 16. Modulo-11 counter

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm SOT109-1

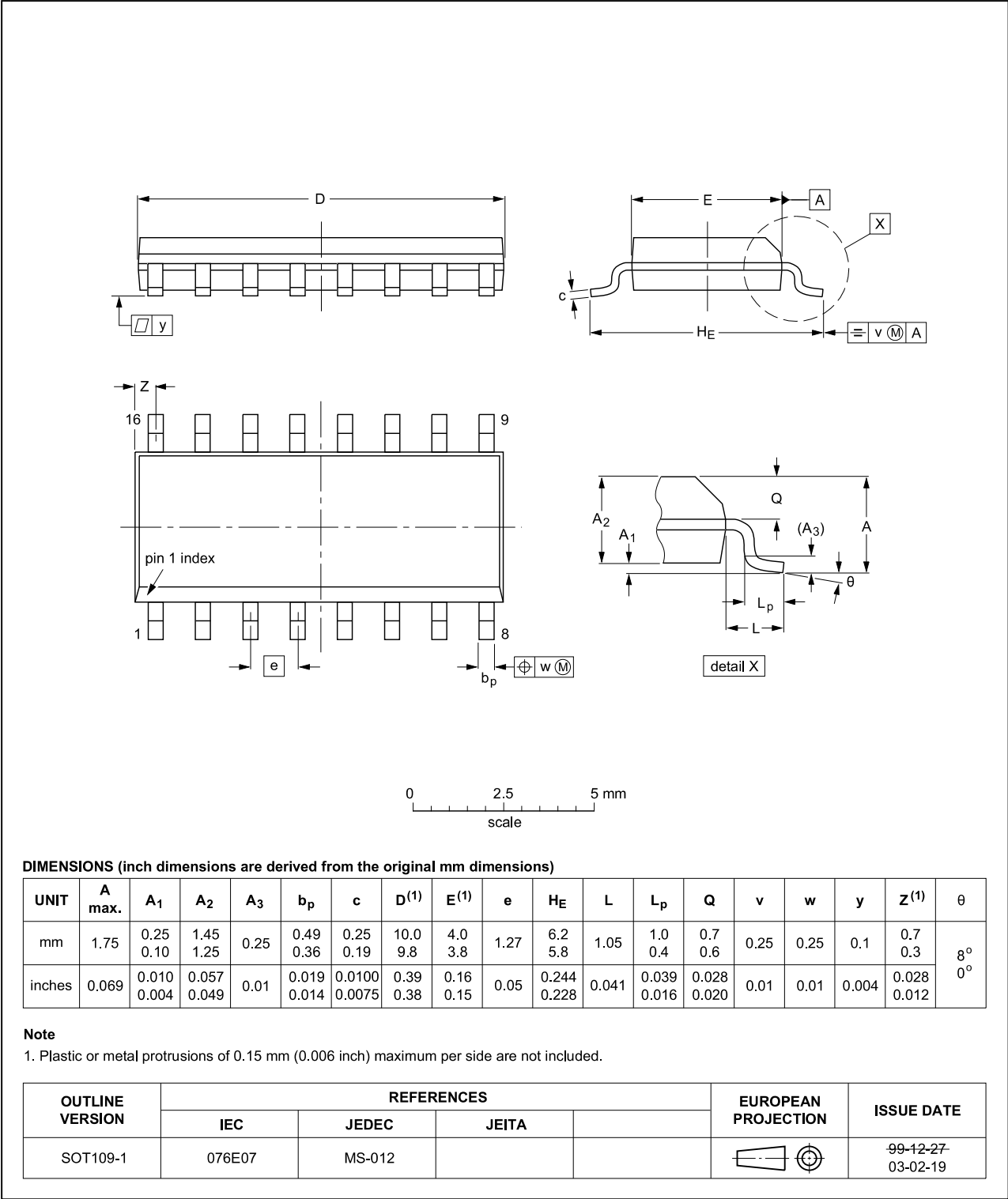
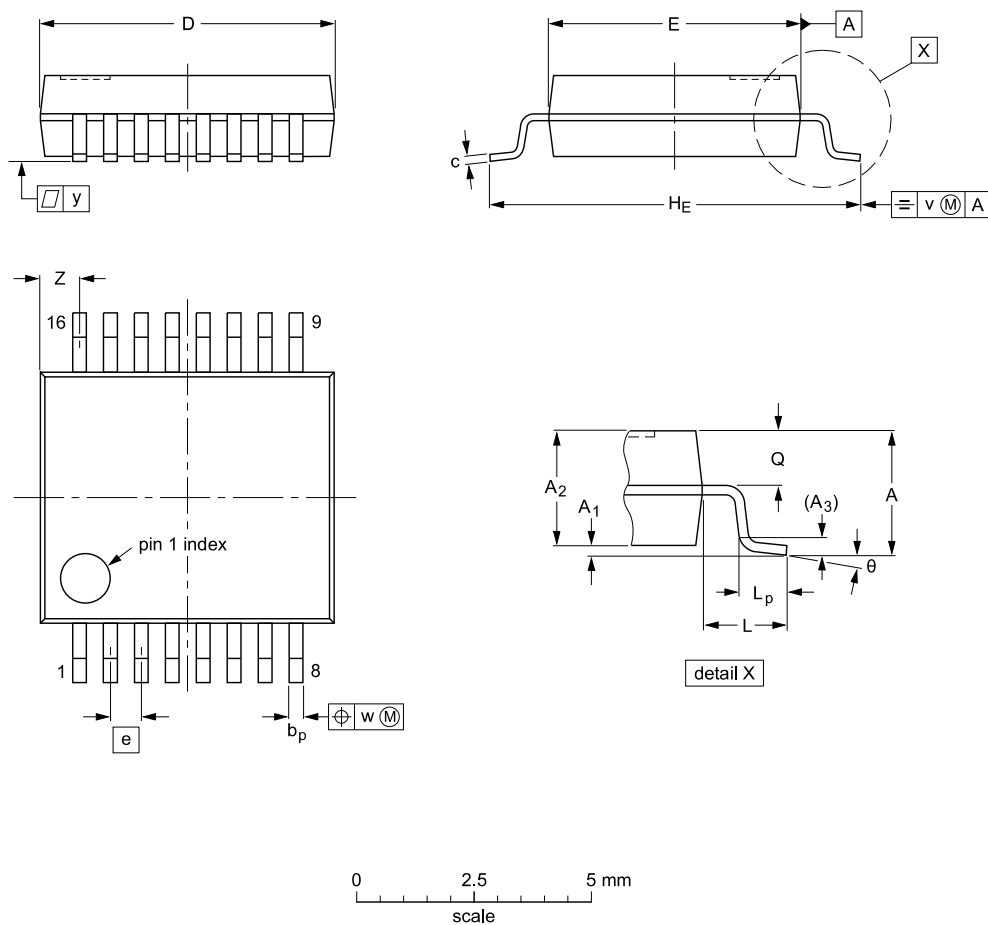


Fig 17. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



DIMENSIONS (mm are the original dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				99-12-27 03-02-19

Fig 18. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

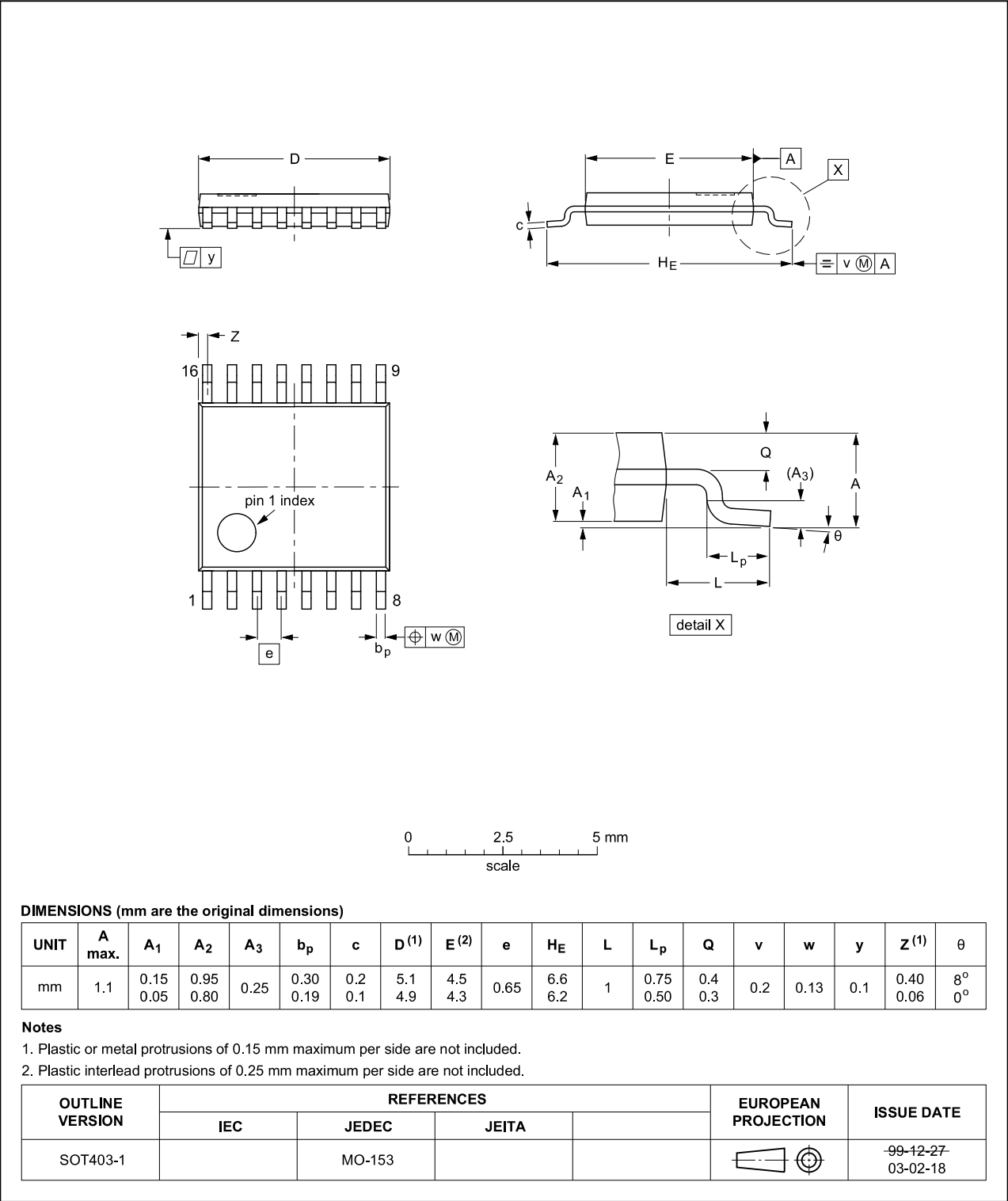


Fig 19. Package outline SOT403-1 (TSSOP16)