LM2940x 1-A Low Dropout Regulator

1 Features

- Input Voltage Range = 6 V to 26 V
- Dropout Voltage Typically 0.5 V at I_{OUT} = 1 A
- Output Current in Excess of 1 A
- Output Voltage Trimmed Before Assembly
- Reverse Battery Protection
- Internal Short Circuit Current Limit
- Mirror Image Insertion Protection
- P^+ Product Enhancement Tested

2 Applications

- Post Regulator for Switching Supplies
- Logic Power Supplies
- Industrial Instrumentation

3 Description

The LM2940-N and LM2940C positive voltage regulators feature the ability to source 1 A of output current with a dropout voltage of typically 0.5 V and a maximum of 1 V over the entire temperature range. Furthermore, a quiescent current reduction circuit has been included which reduces the ground current when the differential between the input voltage and the output voltage exceeds approximately 3 V. The quiescent current with 1 A of output current and an input-output differential of 5 V is therefore only 30 mA. Higher quiescent currents only exist when the regulator is in the dropout mode ($V_{IN} - V_{OUT} \leq 3$ V).

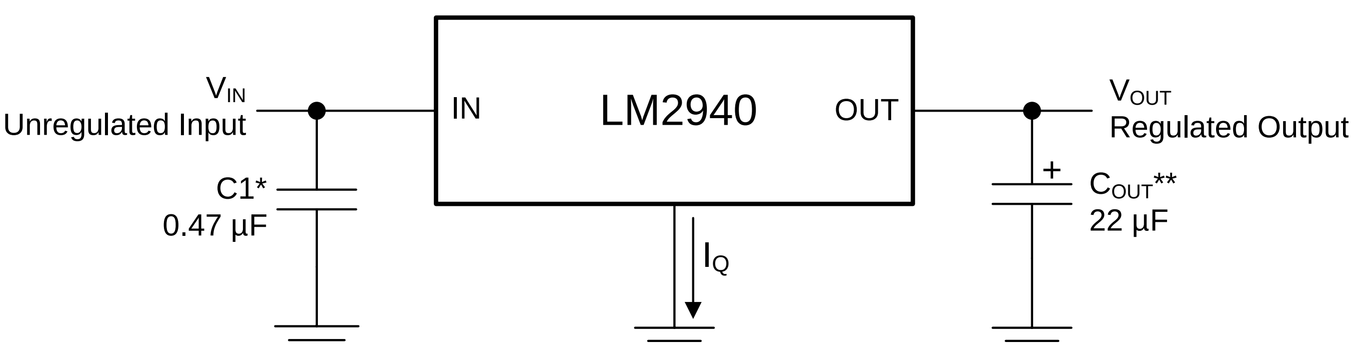
Designed also for vehicular applications, the LM2940-N and LM2940C and all regulated circuitry are protected from reverse battery installations or 2-battery jumps. During line transients, such as load dump when the input voltage can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both the internal circuits and the load. The LM2940-N and LM2940C cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2940-N	SOT-223 (4)	6.50 mm x 3.50 mm
	WSON (8)	4.00 mm x 4.00 mm
	TO-263 (3)	10.18 mm x 8.41 mm
	TO-220 (3)	14.986 mm x 10.16 mm
LM2940C	TO-263 (3)	10.18 mm x 8.41 mm
	TO-220 (3)	14.986 mm x 10.16 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



*Required if regulator is located far from power supply filter.
**C_{OUT} must be at least 22 µF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator and the ESR is critical; see curve.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

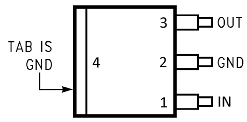
Changes from Revision I (April 2013) to Revision J — **Page**

- Added *Pin Configuration and Functions* section, *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted information re: obsolete CDIP and CLGA package options ; Change pin names from Vin, Vout to IN, OUT; delete Heatsinking sections re: packages apart from TO-220 ... 1
- Changed symbols for Thermal Information ... 19

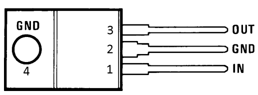
Changes from Revision H (April 2013) to Revision I — **Page**

5 Pin Configuration and Functions

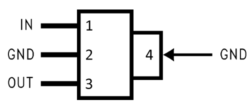
DDPAK/TO-263 (KTT) Package
3 Pins
Top View



TO-220 (NDE) Package
4 Pins
Front View

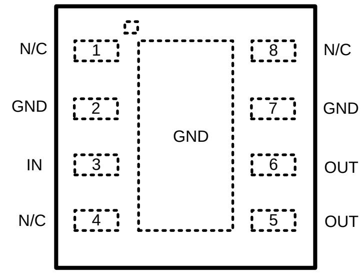


SOT-223 (DCY) Package
3 Pins
Front View



DDPAK/TO-263 (KTT) Package
Side View

WSON (NGN) Package
8 Pins
Top View



Pin 2 and pin 7 are fused to center DAP
Pin 5 and 6 need to be tied together on PCB board

Pin Functions

PIN					I/O	DESCRIPTION
NAME	NDE	KTT	DCY	NGN		
IN	1	1	1	3	I	Unregulated input voltage.
GND	2	2	2	2	—	Ground
OUT	3	3	3	5, 6	O	Regulated output voltage. This pin requires an output capacitor to maintain stability. See *Detailed Design Procedure* for output capacitor details.
GND	4	4	4	7	—	Ground
N/C	—	—	—	1, 4, 8	—	No connection

6 Specifications

6.1 Absolute Maximum Ratings[1][2]

		MIN	MAX	UNIT
LM2940-N KTT, NDE, DCY ≤ 100 ms			60	V
LM2940C KTT, NDE ≤ 1 ms			45	V
Internal power dissipation[3]			Internally Limited	
Maximum junction temperature			150	°C
Soldering temperature[4]	TO-220 (NDE), Wave (10 s)		260	°C
	DDPAK/TO-263 (KTT) (30 s)		235	°C
	SOT-223 (DCY) (30 s)		260	°C
	WSON-8 (NGN) (30 s)		235	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. *Recommended Operating Conditions* are conditions under which the device functions but the specifications might not be ensured. For ensured specifications and test conditions see the *Electrical Characteristics (5 V and 8 V)*.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. The value of $R_{\theta JA}$ (for devices in still air with no heatsink) is 23.3°C/W for the TO-220 package, 40.9°C/W for the DDPAK/TO-263 package, and 59.3°C/W for the SOT-223 package. The effective value of $R_{\theta JA}$ can be reduced by using a heatsink (see *Heatsinking* for specific information on heatsinking). The value of $R_{\theta JA}$ for the WSON package is specifically dependent on PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the WSON package, refer to Application Note AN-1187 *Leadless Leadframe Package (LLP)* (SNOA401). It is recommended that 6 vias be placed under the center pad to improve thermal performance.
(4) Refer to JEDEC J-STD-020C for surface mount device (SMD) package reflow profiles and conditions. Unless otherwise stated, the temperature and time are for Sn-Pb (STD) only.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage		6	26	V
Temperature	LM2940-N NDE, LM2940-N KTT	−40	125	°C
	LM2940C NDE, LM2940C KTT	0	125	°C
	LM2940-N DCY	−40	85	°C
	LM2940-N NGN	−40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LM2940-N, LM2940C		LM2940-N		UNIT
		TO-220 (NDE)	DDPAK/TO-263 (KTT)	SOT-223 (DCY)	WSON (NGN)	
		3 PINS	3 PINS	4 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	23.3	40.9	59.3	40.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.1	43.5	38.9	26.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	4.8	23.5	8.1	17.0	
ψ_{JT}	Junction-to-top characterization parameter	2.7	10.3	1.7	0.2	
ψ_{JB}	Junction-to-board characterization parameter	4.8	22.5	8.0	17.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	0.8	n/a	3.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal information for the TO-220 package is for a package vertically mounted with a heat sink in the middle of a PCB which is compliant to the JEDEC HIGH-K 2s2p (JESD51-7). The heatsink-to-ambient thermal resistance, $R_{\Theta SA}$, is 21.7°C/W. See *Heatsinking TO-220 Package Parts* for more information.

6.5 Electrical Characteristics (5 V and 8 V)

Unless otherwise specified: $V_{IN} = V_{OUT} + 5$ V, $I_{OUT} = 1$ A and $C_{OUT} = 22$ µF. MIN (minimum) and MAX (maximum) limits apply over the recommended operating temperature range, unless otherwise noted; typical limits apply for $T_A = T_J = 25°C$.

PARAMETER	TEST CONDITIONS		5 V			8 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Input voltage	5 mA ≤ I_{OUT} ≤ 1 A		6.25		26	9.4		26	V
Output voltage	5 mA ≤ I_{OUT} ≤ 1A		4.75	5	5.25	7.6	8	8.4	
	5 mA ≤ I_{OUT} ≤ 1A, T_J = 25°C		4.85	5	5.15	7.76	8	8.24	
Line regulation	V_{OUT} + 2 V ≤ V_{IN} ≤ 26 V, I_{OUT} = 5 mA T_J = 25°C			20	50		20	80	mV
Load regulation	50 mA ≤ I_{OUT} ≤ 1 A	LM2940-N		35	80		55	130	mV
	50 mA ≤ I_{OUT} ≤ 1 A T_J = 25°C	LM2940-N		35	50		55	80	
		LM2940C		35	50		55	80	
Output impedance	100 mADC, 20 mArms, f_{OUT} = 120 Hz			35			55		mΩ
Quiescent current	V_{OUT} + 2 V ≤ V_{IN} ≤ 26 V, I_{OUT} = 5 mA	LM2940-N		10	20		10	20	mA
	V_{OUT} + 2 V ≤ V_{IN} ≤ 26 V, I_{OUT} = 5 mA T_J = 25°C	LM2940-N		10	15		10	15	
		LM2940C		10	15				
	$V_{IN} = V_{OUT}$ + 5 V, I_{OUT} = 1 A			30	60		30	60	
	$V_{IN} = V_{OUT}$ + 5 V, I_{OUT} = 1 A T_J = 25°C			30	45		30	45	
Output noise voltage	10 Hz to 100 kHz, I_{OUT} = 5 mA			150			240		µVrms
Ripple rejection	f_{OUT} = 120 Hz, 1 V_{rms}, I_{OUT} = 100 mA	LM2940-N	54	72		48	66		dB
	f_{OUT} = 120 Hz, 1 V_{rms}, I_{OUT} = 100 mA T_J = 25°C	LM2940-N	60	72		54	66		
		LM2940C	60	72		54	66		
Long-term stability				20			32		mV/1000 Hr
Dropout voltage	I_{OUT} = 1A			0.5	1		0.5	1	V
	I_{OUT} = 1A, T_J = 25°C			0.5	0.8		0.5	0.8	
	I_{OUT} = 100 mA			110	200		110	200	mV
	I_{OUT} = 100 mA, T_J = 25°C			110	150		110	150	

Electrical Characteristics (5 V and 8 V) (continued)

Unless otherwise specified: $V_{IN} = V_{OUT} + 5$ V, $I_{OUT} = 1$ A and $C_{OUT} = 22$ µF. MIN (minimum) and MAX (maximum) limits apply over the recommended operating temperature range, unless otherwise noted; typical limits apply for $T_A = T_J = 25°C$.

PARAMETER	TEST CONDITIONS		5 V			8 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Short-circuit current	See(1), $T_J = 25°C$		1.6	1.9		1.6	1.9		A
Maximum line transient	$R_{OUT} = 100\Omega$, T ≤ 100 ms	LM2940-N	60	75		60	75		V
	$R_{OUT} = 100\Omega$, T ≤ 1 ms $T_J = 25°C$	LM2940C	45	55		45	555		
Reverse polarity DC input voltage	$R_{OUT} = 100\ \Omega$	LM2940-N	–15	–30		–15	–30		V
	$R_{OUT} = 100\ \Omega$ $T_J = 25°C$	LM2940C	–15	–30		–15	–30		
Reverse polarity Transient Input Voltage	$R_{OUT} = 100\ \Omega$, T ≤ 100 ms	LM2940-N	–50	–75			–50	–75	V
	$R_{OUT} = 100\ \Omega$, T ≤ 1 ms	LM2940C	–45	–55					

(1) Output current will decrease with increasing temperature but will not drop below 1 A at the maximum specified temperature.

6.6 Electrical Characteristics (9 V and 10 V)

Unless otherwise specified: $V_{IN} = V_{OUT} + 5$ V, $I_{OUT} = 1$ A and $C_{OUT} = 22$ µF. MIN (minimum) and MAX (maximum) limits apply over the recommended operating temperature range, unless otherwise noted; typical limits apply for $T_A = T_J = 25°C$.

PARAMETER	TEST CONDITIONS		9 V			10 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Input voltage	5 mA ≤ I_{OUT} ≤ 1 A		10.5		26	11.5		26	V
Output voltage	5 mA ≤ I_{OUT} ≤ 1A		8.55	9	9.45	9.5	10	10.5	
	5 mA ≤ I_{OUT} ≤ 1A, $T_J = 25°C$		8.73	9	9.27	9.7	10	10.3	
Line regulation	$V_{OUT} + 2$ V ≤ V_{IN} ≤ 26 V, $I_{OUT} = 5$ mA $T_J = 25°C$			20	90		20	100	mV
Load regulation	50 mA ≤ I_{OUT} ≤ 1 A	LM2940-N		60	150		65	165	mV
	50 mA ≤ I_{OUT} ≤ 1 A $T_J = 25°C$	LM2940-N		60	90		65	100	
		LM2940C		60	90				
Output impedance	100 mADC, 20 mArms, $f_{OUT} = 120$ Hz			60			65		mΩ
Quiescent current	$V_{OUT} + 2$ V ≤ V_{IN} ≤ 26 V, $I_{OUT} = 5$ mA	LM2940-N		10	20		10	20	mA
	$V_{OUT} + 2$ V ≤ V_{IN} ≤ 26 V, $I_{OUT} = 5$ mA $T_J = 25°C$	LM2940-N		10	15			15	
		LM2940C		10	15				
	$V_{IN} = V_{OUT} + 5$ V, $I_{OUT} = 1$ A			30	60		30	60	
	$V_{IN} = V_{OUT} + 5$ V, $I_{OUT} = 1$ A $T_J = 25°C$			30	45		30	45	
Output noise voltage	10 Hz to 100 kHz, $I_{OUT} = 5$ mA			270			300		µVrms
Ripple rejection	$f_{OUT} = 120$ Hz, 1 V_{rms} $I_{OUT} = 100$ mA	LM2940-N	46	64		45	63		dB
	$f_{OUT} = 120$ Hz, 1 V_{rms} $I_{OUT} = 100$ mA $T_J = 25°C$	LM2940-N	52	64		51	63		
		LM2940C	52	64					
Long-term stability				34			36		mV/1000 Hr
Dropout voltage	$I_{OUT} = 1A$			0.5	1		0.5	1	V
	$I_{OUT} = 1A$, $T_J = 25°C$			0.5	0.8		0.5	0.8	
	$I_{OUT} = 100$ mA			110	200		110	200	mV
	$I_{OUT} = 100$ mA, $T_J = 25°C$			110	150		110	150	

Electrical Characteristics (9 V and 10 V) (continued)

Unless otherwise specified: $V_{IN} = V_{OUT} + 5$ V, $I_{OUT} = 1$ A and $C_{OUT} = 22$ µF. MIN (minimum) and MAX (maximum) limits apply over the recommended operating temperature range, unless otherwise noted; typical limits apply for $T_A = T_J = 25°C$.

PARAMETER	TEST CONDITIONS		9 V			10 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Short-circuit current	See[1], T_J = 25°C		1.6	1.9		1.6	1.9		A
Maximum line transient	R_{OUT} = 100Ω, T ≤ 100 ms	LM2940-N	60	75		60	75		V
	R_{OUT} = 100Ω, T ≤ 100 ms T_J = 25°C	LM2940C	45	55					
Reverse polarity DC input voltage	R_{OUT} = 100 Ω	LM2940-N	–15	–30		–15	–30		V
	R_{OUT} = 100 Ω T_J = 25°C	LM2940C	–15	–30					
Reverse polarity Transient Input Voltage	R_{OUT} = 100 Ω, T ≤ 100 ms	LM2940-N	–50	–75		–50	–75		V
		LM2940C	–45	–55					

(1) Output current will decrease with increasing temperature but will not drop below 1 A at the maximum specified temperature.

6.7 Electrical Characteristics (12 V and 15 V)

Unless otherwise specified: $V_{IN} = V_{OUT} + 5$ V, $I_{OUT} = 1$ A and $C_{OUT} = 22$ µF. MIN (minimum) and MAX (maximum) limits apply over the recommended operating temperature range, unless otherwise noted; typical limits apply for $T_A = T_J = 25°C$.

PARAMETER	TEST CONDITIONS		12 V			15 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Input voltage	5 mA ≤ I_{OUT} ≤ 1 A		13.6		26	16.75		26	V
Output voltage	5 mA ≤ I_{OUT} ≤ 1A		11.40	12	12.6	14.25	15	15.75	
	5 mA ≤ I_{OUT} ≤ 1A, T_J = 25°C		11.64	12	12.36	14.55	15	15.45	
Line regulation	V_{OUT} + 2 V ≤ V_{IN} ≤ 26 V, I_{OUT} = 5 mA T_J = 25°C			20	120		20	150	mV
Load regulation	50 mA ≤ I_{OUT} ≤ 1 A	LM2940-N		55	200				mV
	50 mA ≤ I_{OUT} ≤ 1 A T_J = 25°C	LM2940-N		55	120				
		LM2940C		55	120		70	150	
Output impedance	100 mADC, 20 mArms, f_{OUT} = 120 Hz			80			100		mΩ
Quiescent current	V_{OUT} + 2 V ≤ V_{IN} ≤ 26 V, I_{OUT} = 5 mA	LM2940-N		10	20				mA
	V_{OUT} + 2 V ≤ V_{IN} ≤ 26 V, I_{OUT} = 5 mA T_J = 25°C	LM2940-N		10	15				
		LM2940C		10	15		10	15	
	V_{IN} = V_{OUT} + 5 V, I_{OUT} = 1 A			30	60		30	60	
	V_{IN} = V_{OUT} + 5 V, I_{OUT} = 1 A T_J = 25°C			30	45		30	45	
Output noise voltage	10 Hz to 100 kHz, I_{OUT} = 5 mA			360			450		µVrms
Ripple rejection	f_{OUT} = 120 Hz, 1 V_{rms}, I_{OUT} = 100 mA	LM2940-N	48	66					dB
	f_{OUT} = 120 Hz, 1 V_{rms}, I_{OUT} = 100 mA T_J = 25°C	LM2940-N	54	66					
		LM2940C	54	66		52	64		
Long-term stability				48			60		mV/1000 Hr
Dropout voltage	I_{OUT} = 1A			0.5	1		0.5	1	V
	I_{OUT} = 1A, T_J = 25°C			0.5	0.8		0.5	0.8	
	I_{OUT} = 100 mA			110	200		110	200	mV
	I_{OUT} = 100 mA, T_J = 25°C			110	150		110	150	

Electrical Characteristics (12 V and 15 V) (continued)

Unless otherwise specified: $V_{IN} = V_{OUT} + 5$ V, $I_{OUT} = 1$ A and $C_{OUT} = 22$ µF. MIN (minimum) and MAX (maximum) limits apply over the recommended operating temperature range, unless otherwise noted; typical limits apply for $T_A = T_J = 25°C$.

PARAMETER	TEST CONDITIONS		12 V MIN	12 V TYP	12 V MAX	15 V MIN	15 V TYP	15 V MAX	UNIT
Short-circuit current	See[(1)], $T_J = 25°C$		1.6	1.9		1.6	1.9		A
Maximum line transient	$R_{OUT} = 100Ω$, T ≤ 100 ms	LM2940-N	60	75					V
	$R_{OUT} = 100Ω$, T ≤ 100 ms $T_J = 25°C$	LM2940C	45	55		45	55		
Reverse polarity DC input voltage	$R_{OUT} = 100$ Ω	LM2940-N	–15	–30					V
	$R_{OUT} = 100$ Ω $T_J = 25°C$	LM2940C	–15	–30		–15	–30		
Reverse polarity transient input voltage	$R_{OUT} = 100$ Ω, T ≤ 100 ms	LM2940-N	–50	–75					V
	$R_{OUT} = 100$ Ω, T ≤ 1 ms	LM2940C	–45	–55		–45	–55		

(1) Output current will decrease with increasing temperature but will not drop below 1 A at the maximum specified temperature.

6.8 Typical Characteristics

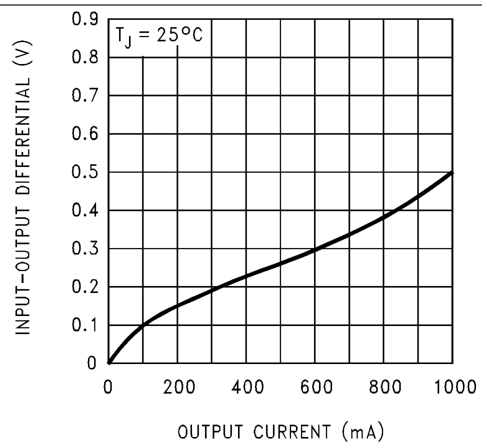


Figure 1. Dropout Voltage

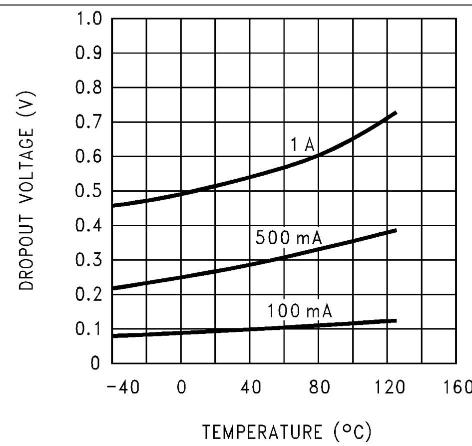


Figure 2. Dropout Voltage vs. Temperature

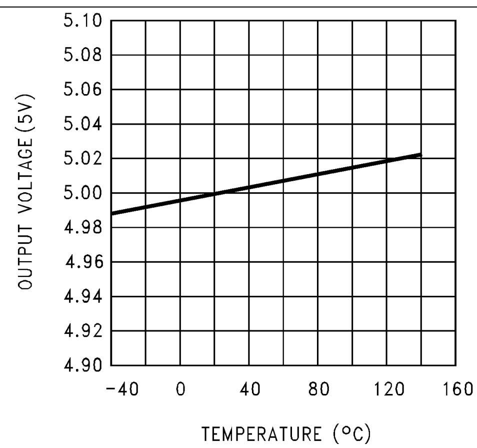


Figure 3. Output Voltage vs. Temperature

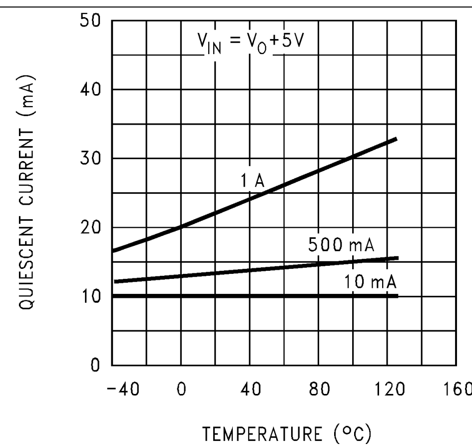


Figure 4. Quiescent Current vs. Temperature

Typical Characteristics (continued)

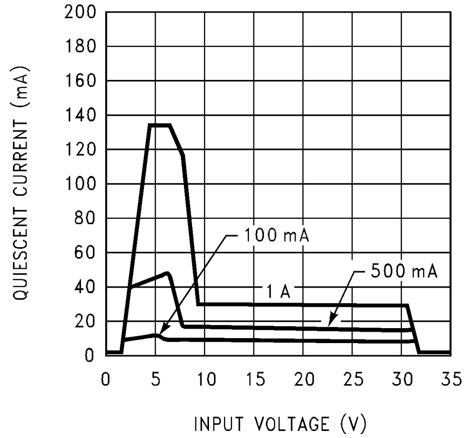


Figure 5. Quiescent Current

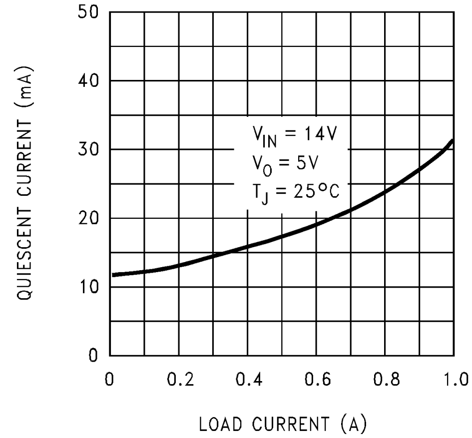


Figure 6. Quiescent Current

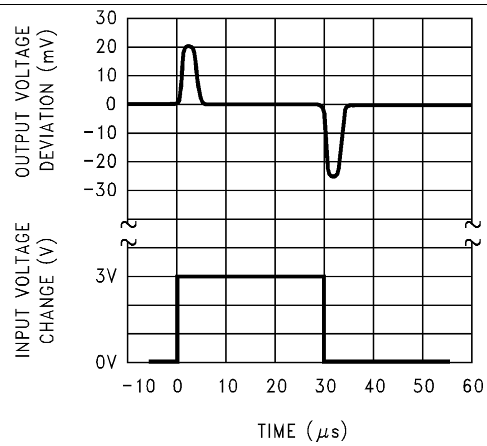


Figure 7. Line Transient Response

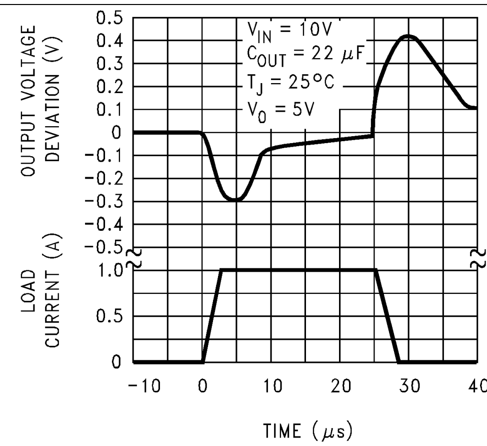


Figure 8. Load Transient Response

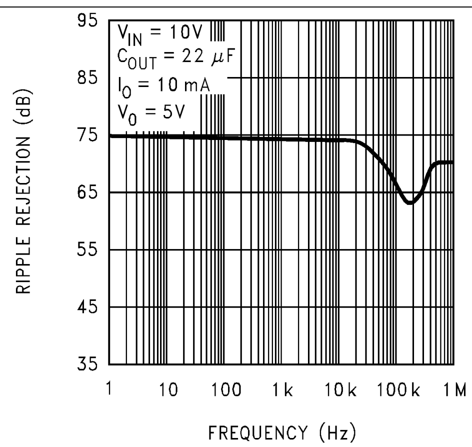


Figure 9. Ripple Rejection

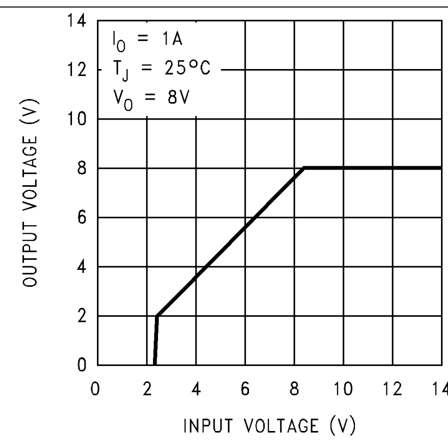


Figure 10. Low Voltage Behavior

Typical Characteristics (continued)

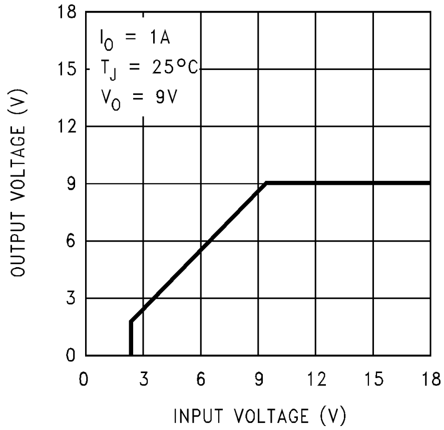


Figure 11. Low Voltage Behavior

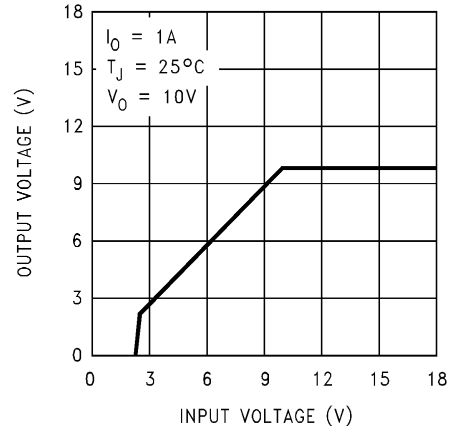


Figure 12. Low Voltage Behavior

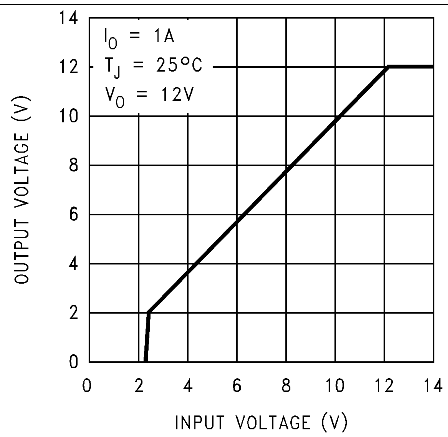


Figure 13. Low Voltage Behavior

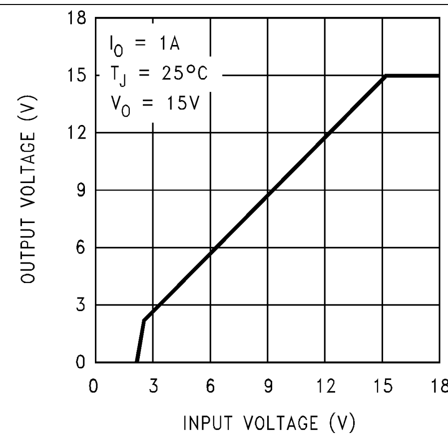


Figure 14. Low Voltage Behavior

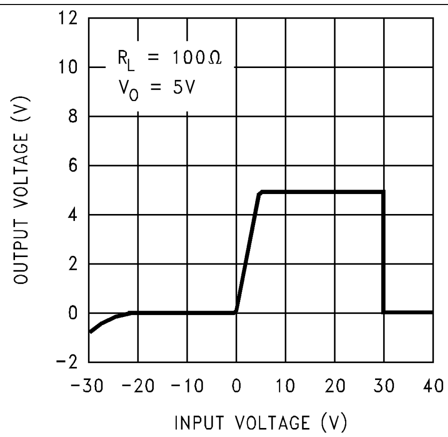


Figure 15. Output at Voltage Extremes

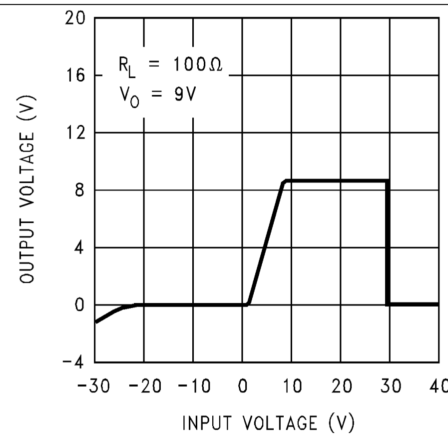


Figure 16. Output at Voltage Extremes

Typical Characteristics (continued)

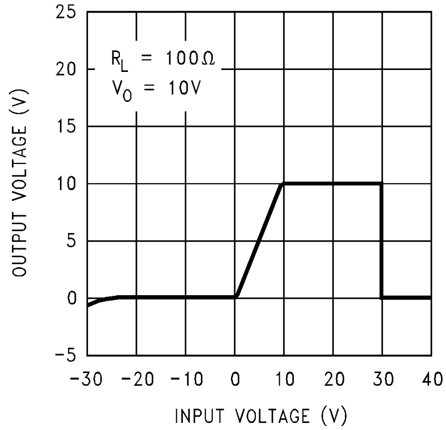


Figure 17. Output at Voltage Extremes

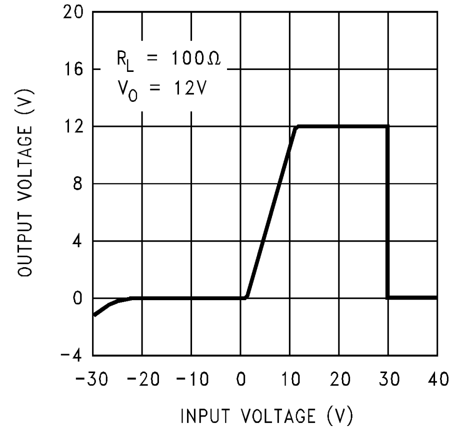


Figure 18. Output at Voltage Extremes

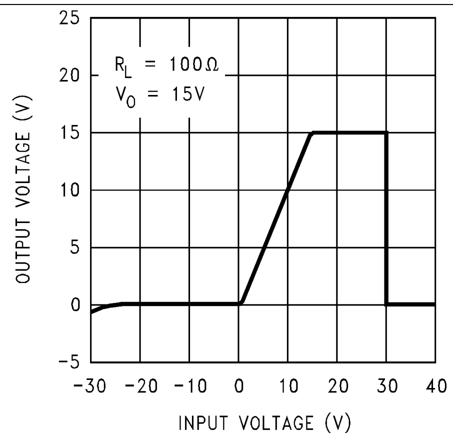


Figure 19. Output at Voltage Extremes

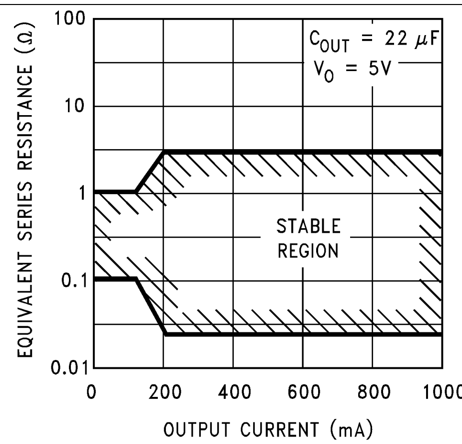


Figure 20. Output Capacitor ESR

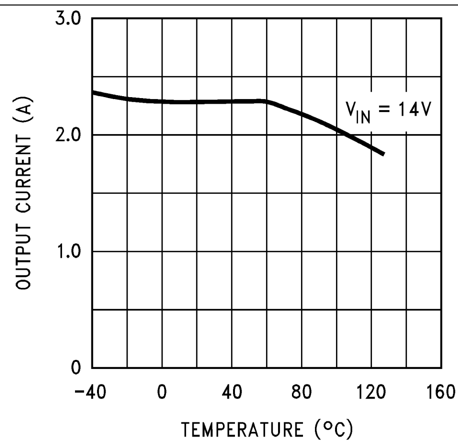


Figure 21. Peak Output Current

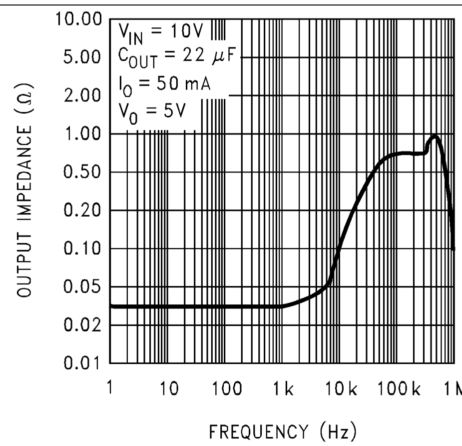


Figure 22. Output Impedance

Typical Characteristics (continued)

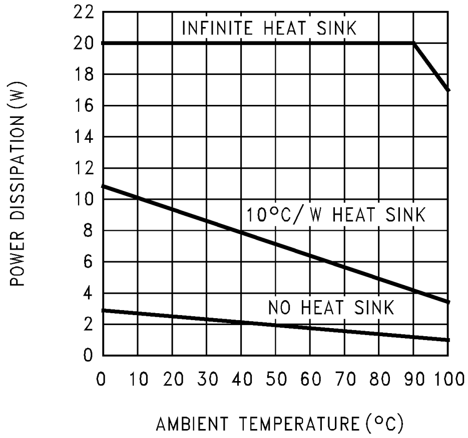


Figure 23. Maximum Power Dissipation (TO-220)

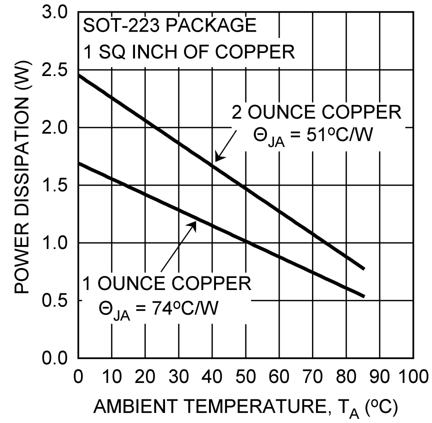


Figure 24. Maximum Power Dissipation (SOT-223)

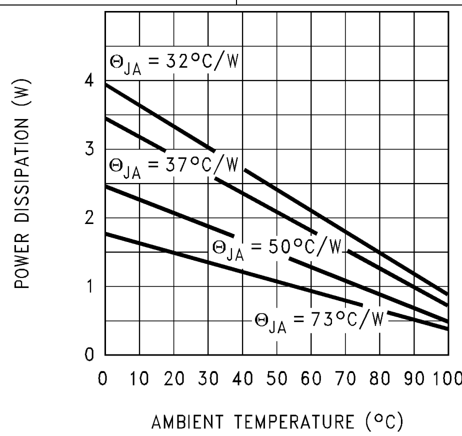


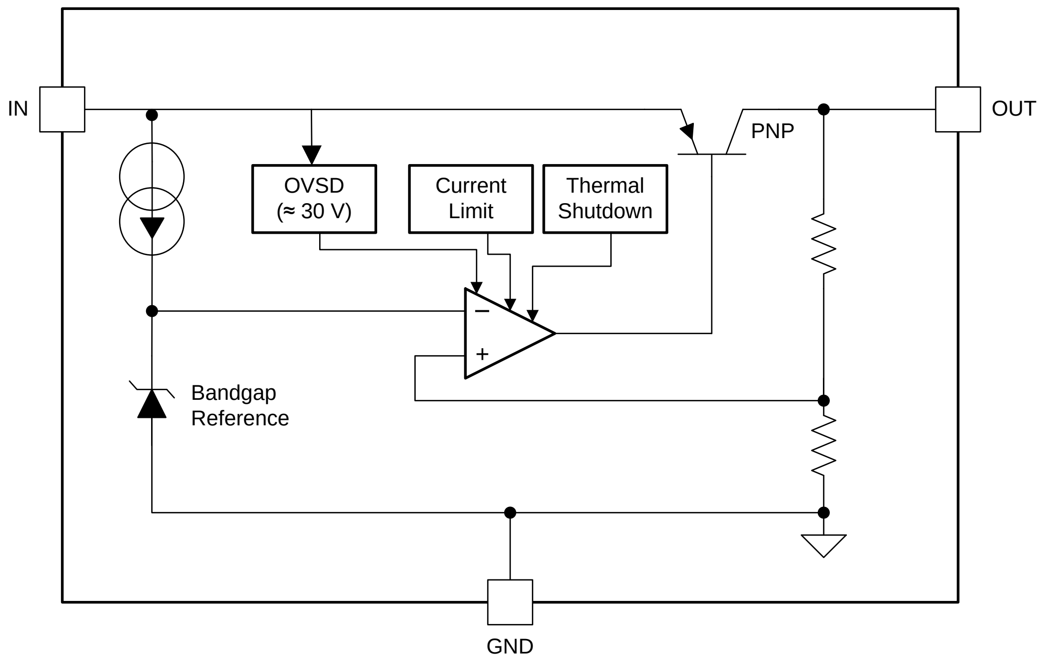
Figure 25. Maximum Power Dissipation (DDPAK/TO-263)

7 Detailed Description

7.1 Overview

The LM2940 positive voltage regulator features the ability to source 1 A of output current with a dropout voltage of typically 0.5 V and a maximum of 1 V over the entire temperature range. Furthermore, a quiescent current reduction circuit has been included which reduces the ground current when the differential between the input voltage and the output voltage exceeds approximately 3 V. The quiescent current with 1 A of output current and an input-output differential of 5 V is therefore only 30 mA. Higher quiescent currents only exist when the regulator is in the dropout mode (V_{IN} – V_{OUT} ≤ 3 V).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Short-Circuit Current Limit

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. Note, also, that if a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO, resulting a thermal shutdown of the output.

7.3.2 Overvoltage Shutdown (OVSD)

Input voltage greater than typically 30 V will cause the LM2940 output to be disabled. When operating with the input voltage greater than the maximum recommended input voltage of 26 V, the device performance is not ensured. Continuous operation with the input voltage greater than the maximum recommended input voltage is discouraged.

7.3.3 Thermal Shutdown (TSD)

The LM2940 contains the thermal shutdown circuitry to turn off the output when excessive heat is dissipated in the LDO. The internal protection circuitry of the LM2940 is designed to protect against thermal overload conditions. The TSD circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown degrades its reliability as the junction temperature will be exceeding the absolute maximum junction temperature rating.

7.4 Device Functional Modes

7.4.1 Operation with Enable Control

The LM2940 design does not include any undervoltage lockout (UVLO), or enable functions. Generally, the output voltage will track the input voltage until the input voltage is greater than V_{OUT} + 1V. When the input voltage is greater than V_{OUT} + 1 V, the LM2940 will be in linear operation, and the output voltage will be regulated. However, the device will be sensitive to any small perturbation of the input voltage. Device dynamic performance is improved when the input voltage is at least 2 V greater than the output voltage.

8 Application and Implementation

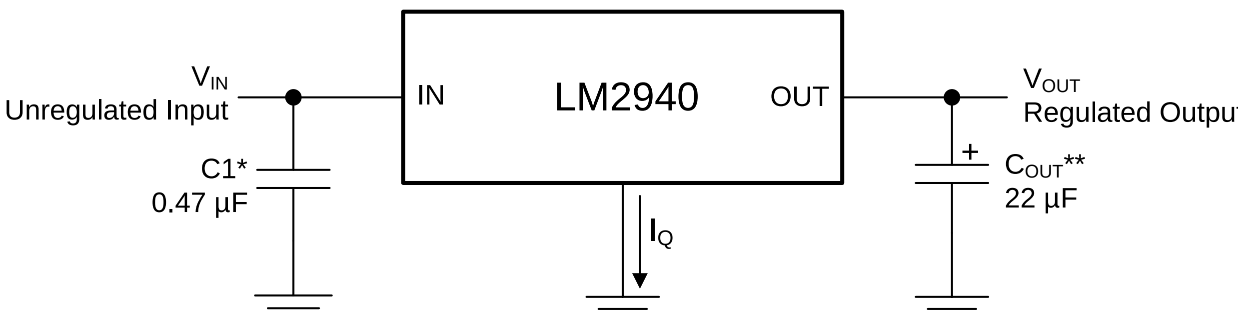
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM2940-N and LM2940C positive voltage regulators feature the ability to source 1 A of output current with a dropout voltage of typically 0.5 V and a maximum of 1 V over the entire temperature range. The output capacitor, C_{OUT}, must have a capacitance value of at least 22 µF with an ESR of at least 100 mΩ, but no more than 1 Ω. The minimum capacitance value and the ESR requirements apply across the entire expected operating ambient temperature range.

8.2 Typical Application



*Required if regulator is located far from power supply filter.
**C_{OUT} must be at least 22 µF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator and the ESR is critical; see curve.

Figure 26. Typical Application

8.2.1 Design Requirements

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	6 V to 26 V
Output voltage range	8 V
Output current range	5 mA to 1 A
Input capacitor value	0.47 µF
Output capacitor value	22 µF minimum
Output capacitor ESR range	100 mΩ to 1 Ω

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

The output capacitor is critical to maintaining regulator stability, and must meet the required conditions for both equivalent series resistance (ESR) and minimum amount of capacitance.

8.2.2.1.1 Minimum Capacitance

The minimum output capacitance required to maintain stability is 22 µF (this value may be increased without limit). Larger values of output capacitance will give improved transient response.

8.2.2.1.2 ESR Limits

The ESR of the output capacitor will cause loop instability if it is too high or too low. The acceptable range of ESR plotted versus load current is shown in the graph below. *It is essential that the output capacitor meet these requirements, or oscillations can result.*

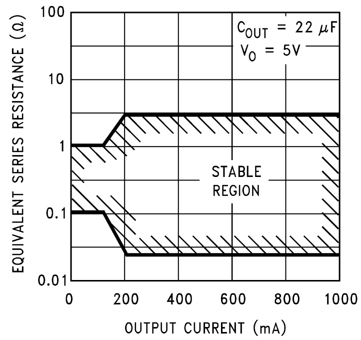


Figure 27. Output Capacitor ESR Limits

It is important to note that for most capacitors, ESR is specified only at room temperature. However, the designer must ensure that the ESR will stay inside the limits shown over the entire operating temperature range for the design.

For aluminum electrolytic capacitors, ESR will increase by about 30X as the temperature is reduced from 25°C to −40°C. This type of capacitor is not well-suited for low temperature operation.

Solid tantalum capacitors have a more stable ESR over temperature, but are more expensive than aluminum electrolytics. A cost-effective approach sometimes used is to parallel an aluminum electrolytic with a solid tantalum, with the total capacitance split about 75/25% with the aluminum being the larger value.

If two capacitors are paralleled, the effective ESR is the parallel of the two individual values. The flatter ESR of the tantalum will keep the effective ESR from rising as quickly at low temperatures.

8.2.3 Application Curves

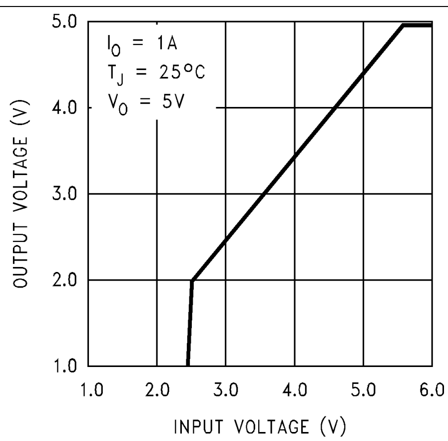


Figure 28. Low Voltage Behavior

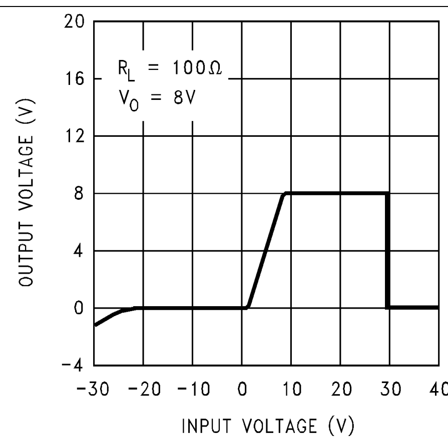


Figure 29. Output at Voltage Extremes

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between V_{OUT} + 1 V up to a maximum of 26 V. This input supply must be well regulated and free of spurious noise. To ensure that the LM2940 output voltage is well regulated, the input supply should be at least V_{OUT} + 2 V.

10 Layout

10.1 Layout Guidelines

The dynamic performance of the LM2940 is dependent on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LM2940. Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LM2940, and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} should be back to the LM2940 ground pin using as wide and short of a copper trace as is practical.

10.2 Layout Examples

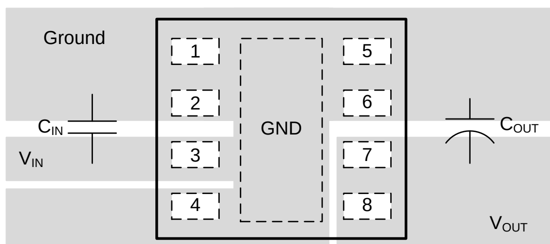


Figure 30. LM2940 WSON Layout

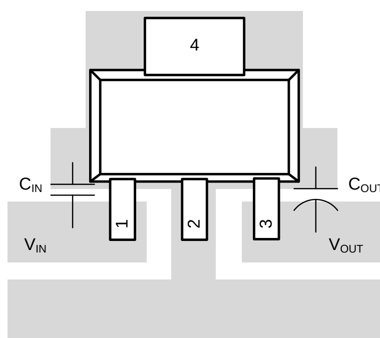


Figure 31. LM2940 SOT-223 Layout

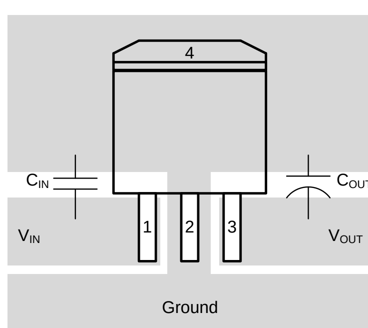


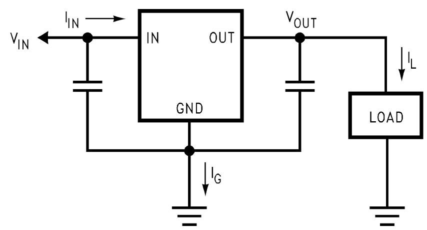
Figure 32. TO-263 Layout

10.3 Heatsinking

A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible operating conditions, the junction temperature must be within the range specified under *Absolute Maximum Ratings*[(1)(2)].

To determine if a heatsink is required, the power dissipated by the regulator, P_D, must be calculated.

Figure 33 shows the voltages and currents which are present in the circuit, as well as the formula for calculating the power dissipated in the regulator:



$I_{IN} = I_L + I_G$
$P_D = (V_{IN} - V_{OUT})\ I_L + (V_{IN})\ I_G$

Figure 33. Power Dissipation Diagram

The next parameter which must be calculated is the maximum allowable temperature rise, $T_{R(MAX)}$. This is calculated by using the formula:

$T_{R(MAX)} = T_{J(MAX)} - T_{A(MAX)}$

where

- $T_{J(MAX)}$ is the maximum allowable junction temperature, which is 125°C for commercial grade parts.
- $T_{A(MAX)}$ is the maximum ambient temperature which will be encountered in the application. (1)

Using the calculated values for $T_{R(MAX)}$ and P_D, the maximum allowable value for the junction-to-ambient thermal resistance, $R_{\theta JA}$, can now be found:

$R_{\theta JA} = T_{R(MAX)} / P_D$ (2)

NOTE

If the maximum allowable value for $R_{\theta JA}$ is found to be ≥ 23.3°C/W for the TO-220 package (with a heatsink of 21.7°C/W $R_{\theta SA}$), ≥ 40.9°C/W for the DDPAK/TO-263 package, or ≥ 59.3°C/W for the SOT-223 package, no heatsink is needed since the package alone will dissipate enough heat to satisfy these requirements.

If the calculated value for $R_{\theta JA}$ falls below these limits, a heatsink is required.

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. *Recommended Operating Conditions* are conditions under which the device functions but the specifications might not be ensured. For ensured specifications and test conditions see the *Electrical Characteristics (5 V and 8 V)*.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Heatsinking (continued)

10.3.1 Heatsinking TO-220 Package Parts

The TO-220 can be attached to a typical heatsink, or secured to a copper plane on a PC board.

If a manufactured heatsink is to be selected, the value of heatsink-to-ambient thermal resistance, $R_{\theta SA}$, must first be calculated:

$$R_{\theta SA} = R_{\theta JA} - R_{\theta CS} - R_{\theta JC} \quad (3)$$

where

- $R_{\theta JC}$ is defined as the thermal resistance from the junction to the surface of the case. A value of 3°C/W can be assumed for $R_{\theta JC}$ for this calculation.
- $R_{\theta CS}$ is defined as the thermal resistance between the case and the surface of the heatsink. The value of $R_{\theta CS}$ will vary from about 0.5°C/W to about 2.5°C/W (depending on method of attachment, insulator, etc.). If the exact value is unknown, 2°C/W should be assumed for $R_{\theta CS}$. (3)

When a value for $R_{\theta SA}$ is found using Equation 3, *a heatsink must be selected that has a value that is less than or equal to this number.*

$R_{\theta SA}$ is specified numerically by the heatsink manufacturer in the catalog, or shown in a curve that plots temperature rise vs power dissipation for the heatsink.

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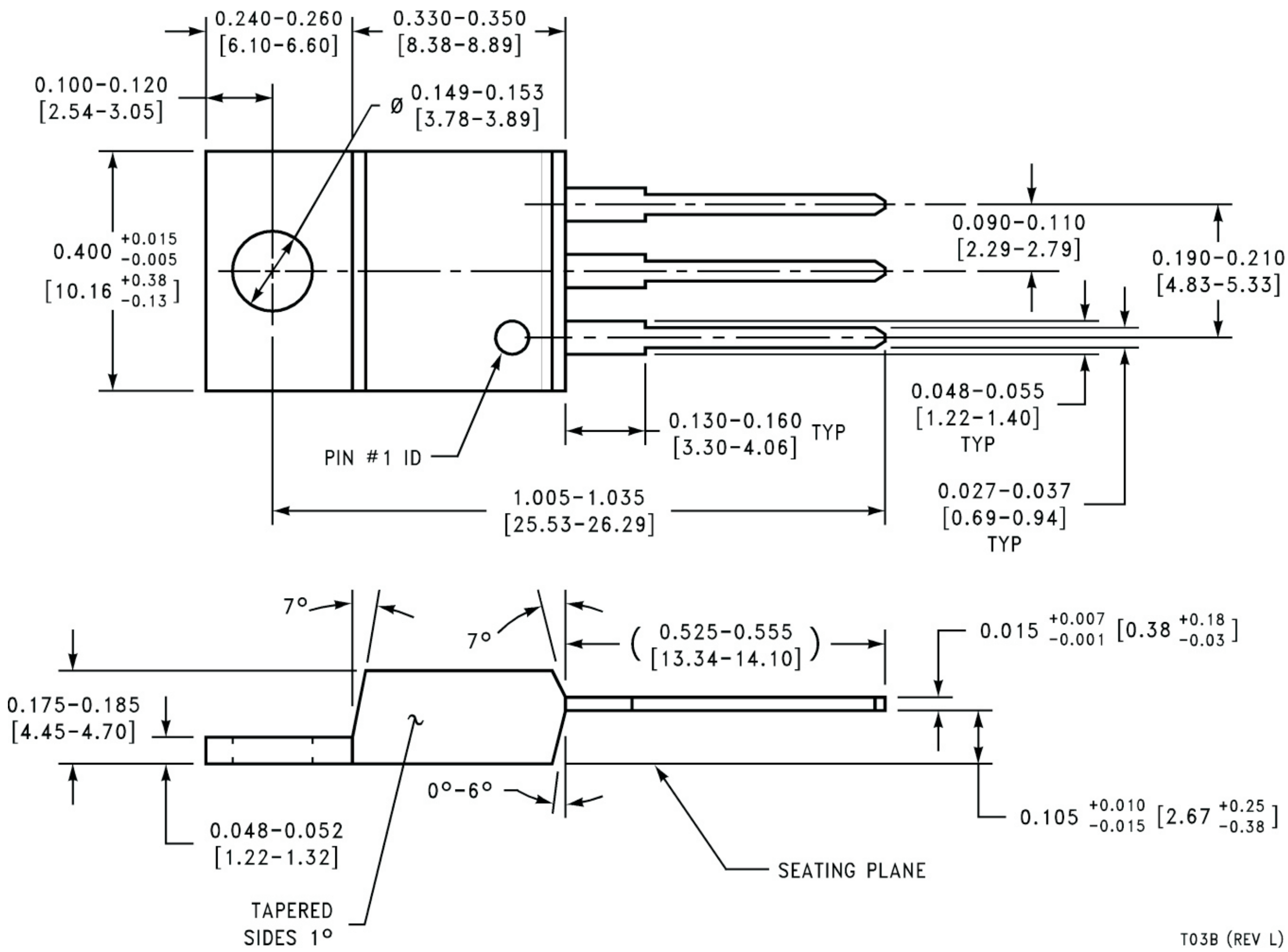
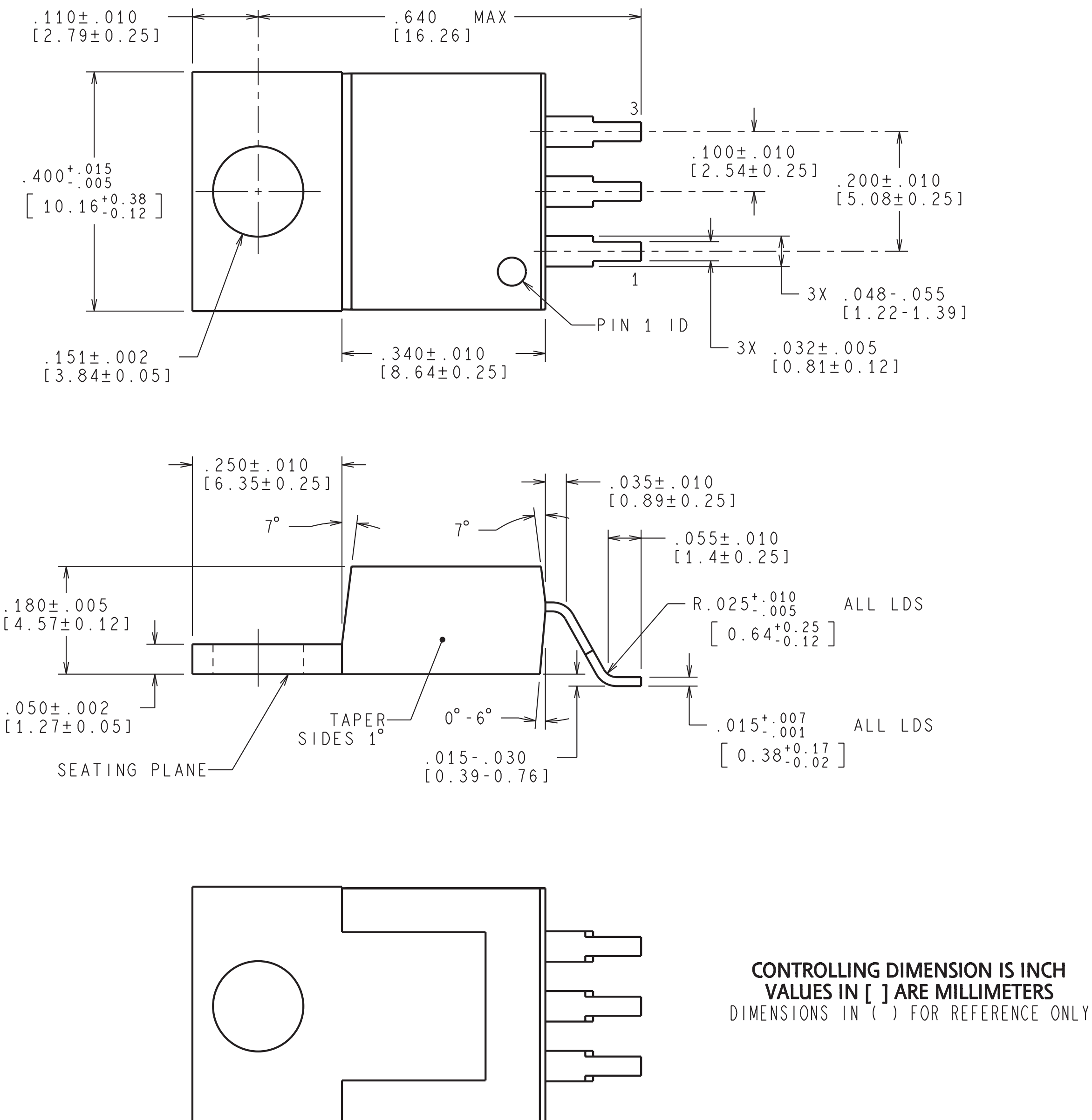
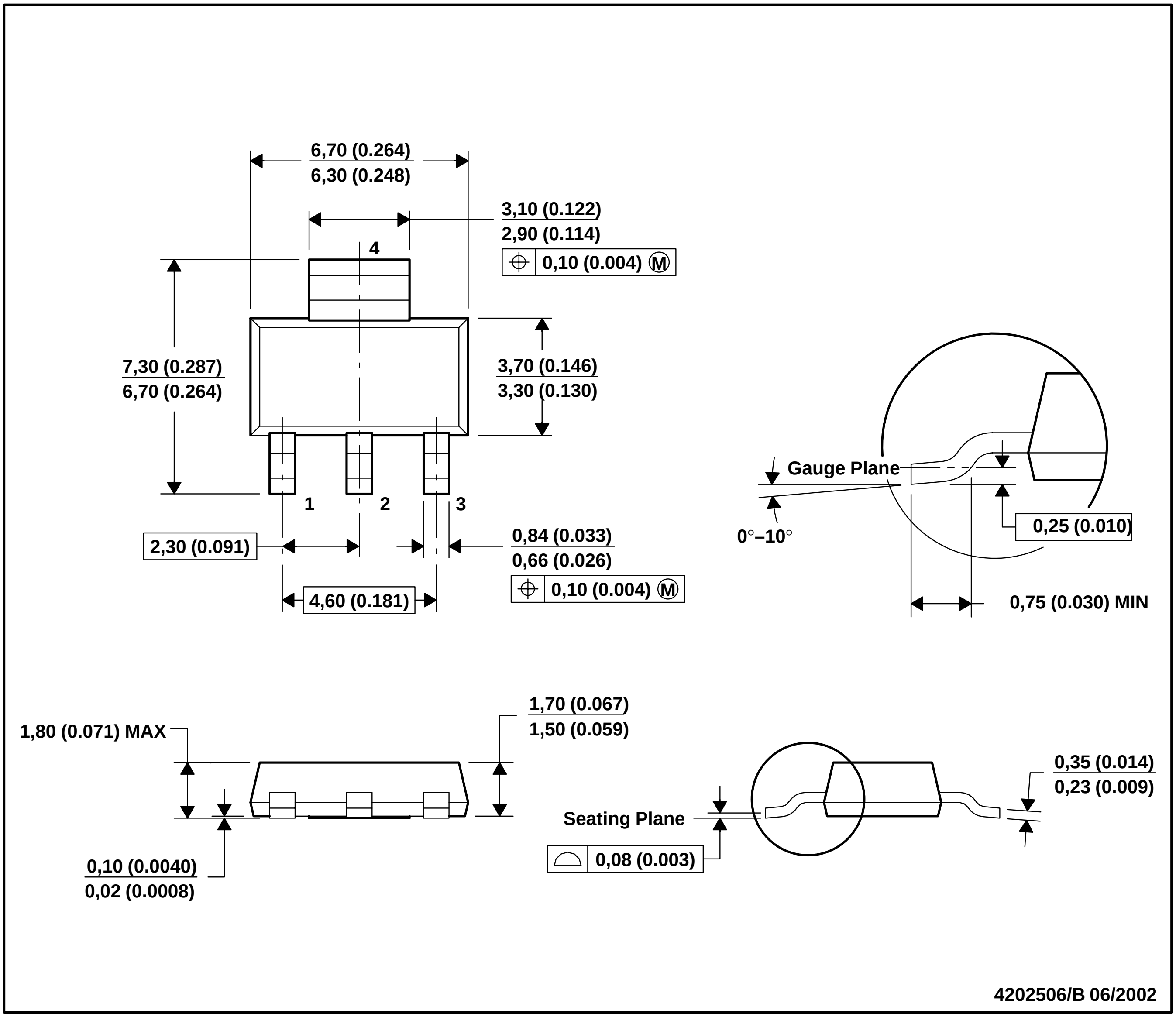

0.240–0.260
[6.10–6.60]
0.330–0.350
[8.38–8.89]
0.100–0.120
[2.54–3.05]
Ø 0.149–0.153
[3.78–3.89]
0.400 +0.015 −0.005
[10.16 +0.38 −0.13]
0.090–0.110
[2.29–2.79]
0.190–0.210
[4.83–5.33]
0.048–0.055
[1.22–1.40]
TYP
0.130–0.160 TYP
[3.30–4.06]
PIN #1 ID
1.005–1.035
[25.53–26.29]
0.027–0.037
[0.69–0.94]
TYP
7°
7°
(0.525–0.555
[13.34–14.10])
0.015 +0.007 −0.001 [0.38 +0.18 −0.03]
0.175–0.185
[4.45–4.70]
0°–6°
0.048–0.052
[1.22–1.32]
0.105 +0.010 −0.015 [2.67 +0.25 −0.38]
SEATING PLANE
TAPERED
SIDES 1°
T03B (REV L)

NDG0003F



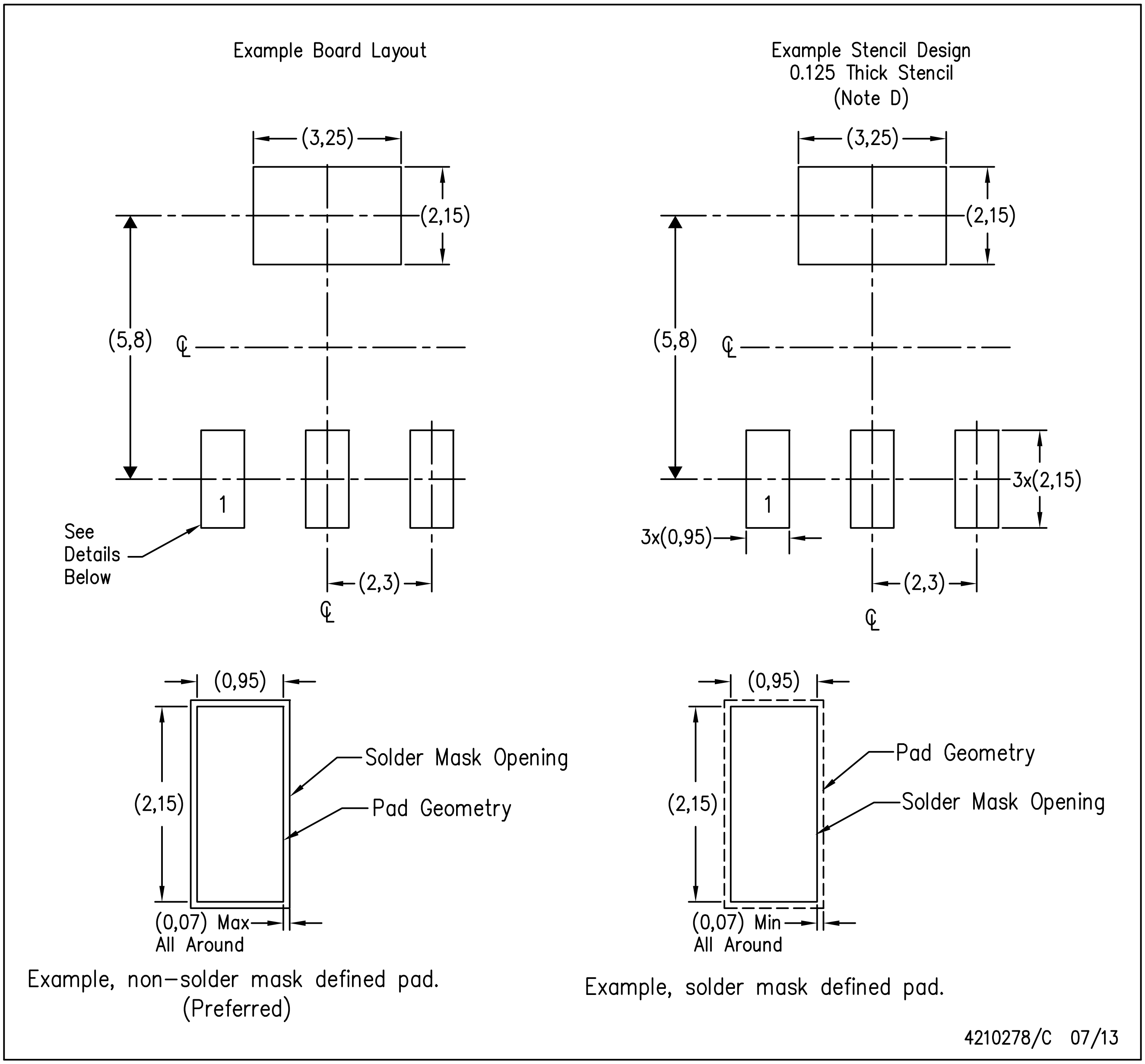
T03F (Rev B)

DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

DCY (R–PDSO–G4) PLASTIC SMALL OUTLINE



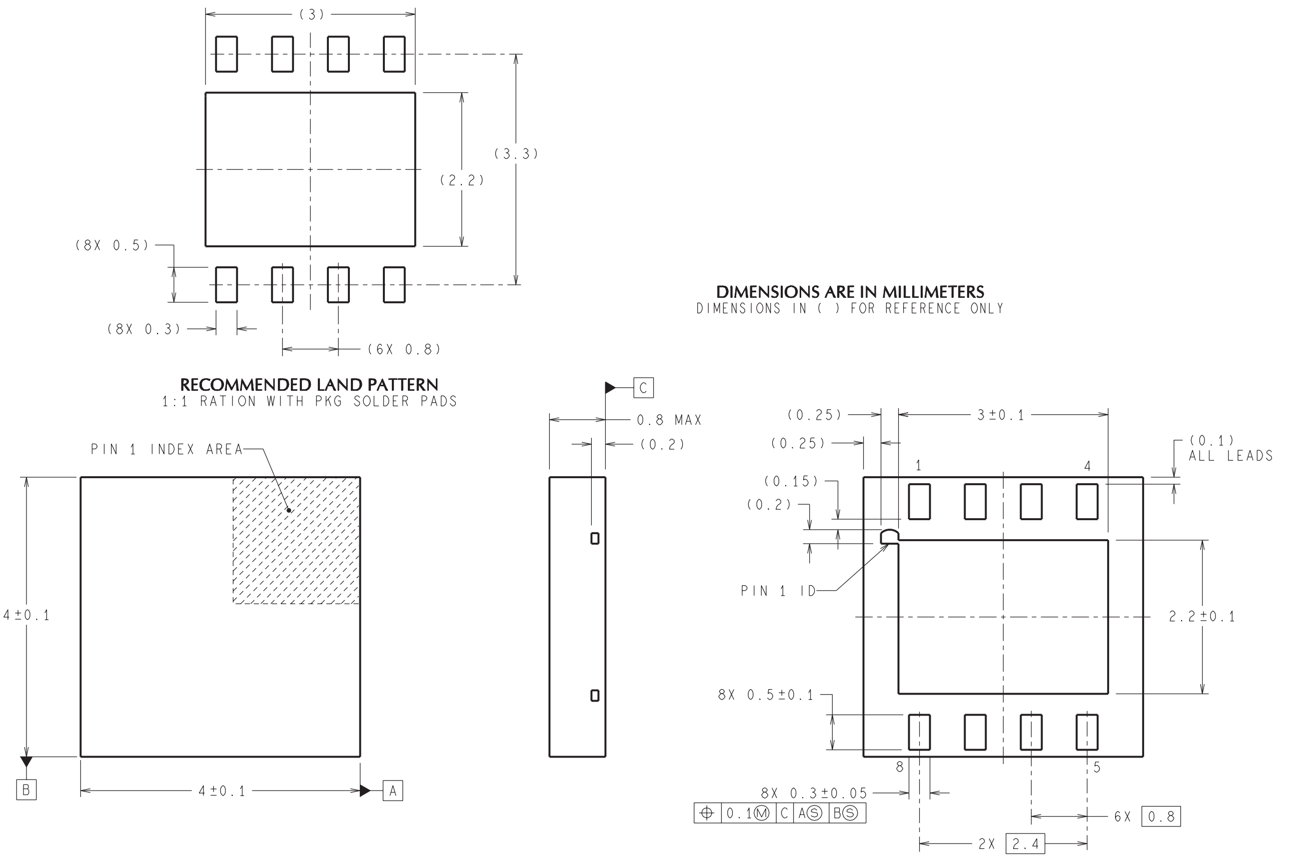
NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Publication IPC–7351 is recommended for alternate designs.

D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil recommendations. Refer to IPC 7525 for stencil design considerations.


(3)
(3.3)
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(8X 0.5)
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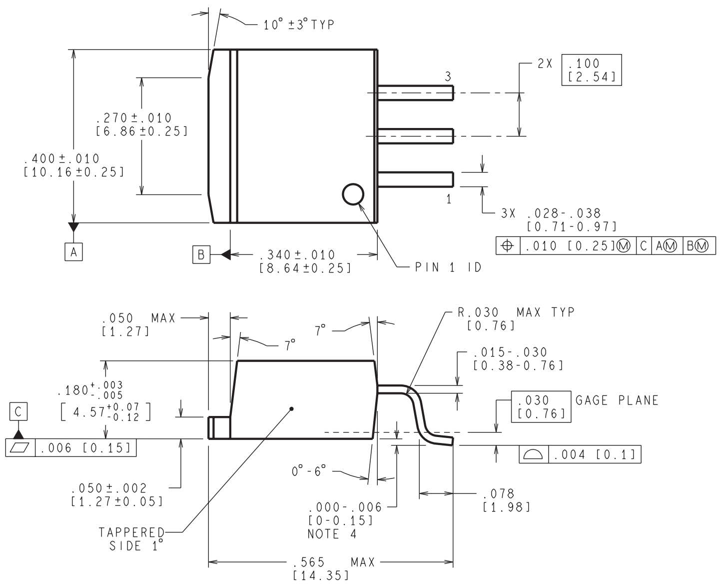
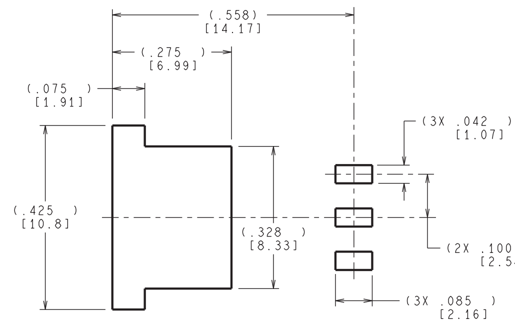
(6X 0.8)
RECOMMENDED LAND PATTERN
1:1 RATION WITH PKG SOLDER PADS
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY
PIN 1 INDEX AREA
4±0.1
4±0.1
B
A
C
0.8 MAX
(0.2)
(0.25)
(0.25)
3±0.1
(0.1)
ALL LEADS
(0.15)
(0.2)
1
4
PIN 1 ID
2.2±0.1
8X 0.5±0.1
8
5
8X 0.3±0.05
0.1 M C A S B S
6X 0.8
2X 2.4

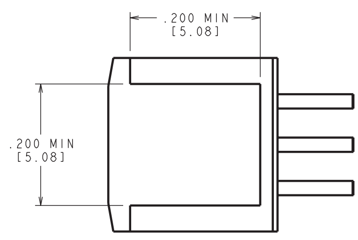
LDC08A (Rev B)

KTT0003B





LAND PATTERN RECOMMENDATION



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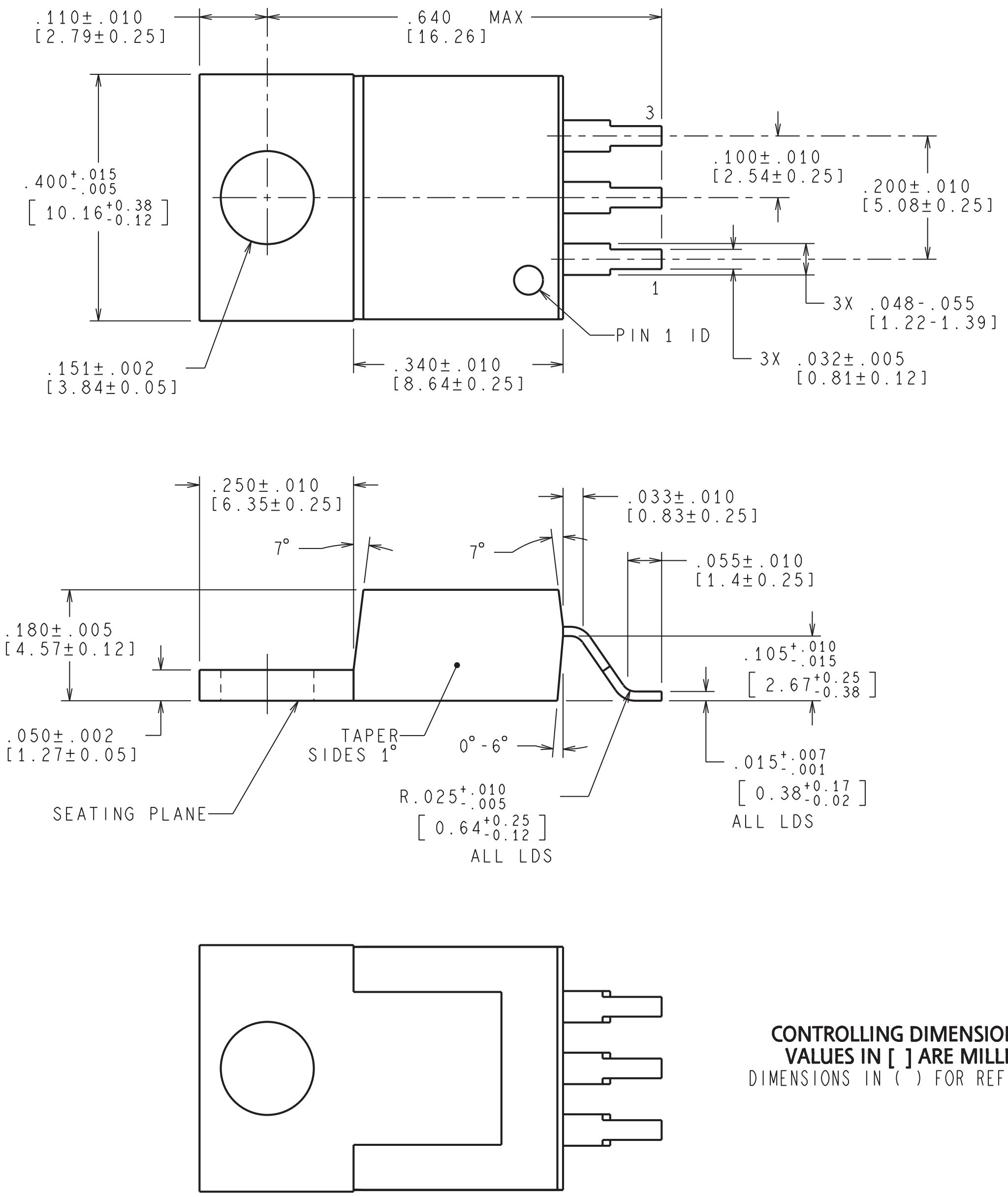
BOTTOM SIDE OF PACKAGE

TS3B (Rev F)

NEB0003G



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TA03G (Rev A)