# UM5100

## Voice Processor

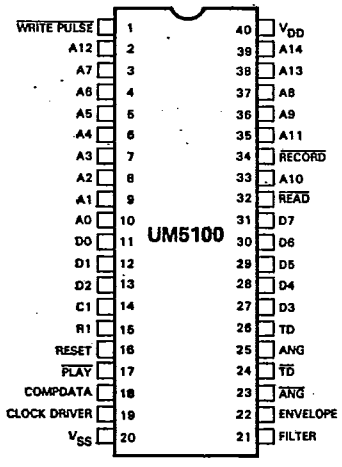
### Features

- Voice recording and reproduction with external SRAM
- Voice reproduction with external EPROM or ROM
- Continuous variable slope Delta Modulation
- Max. addressable memory 256K
- Single 3V ~ 6V power operation
- Low power consumption by CMOS structure
- Inexpensive RC oscillation
- Adjustable bit rates from 10K to 28K bps.
- High quality voice reproduction
- Application for voice storage, security system, telecommunication and other voice fields

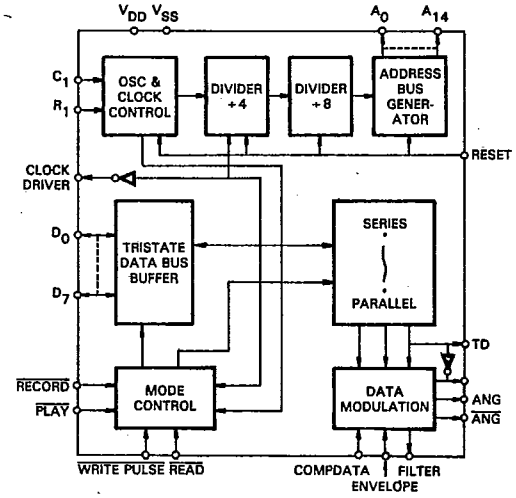
### General Description

The UM5100 is a single chip CMOS LSI for voice recording and reproduction with SRAM or voice only production with EPROM or ROM. It is composed of RC oscillator, Address/data bus, series to parallel (and vice versa) converter, mode controller and delta modulation. The Delta modulation circuit is based on a continuous variable slope waveform by digital recording and reproduction of voice signals. For low frequency, there are auxiliary outputs to avoid distortion. For high frequency, there is an internal amplifier, to intensify voice loudness. The RC oscillator is the best option in bit rates from 10K to 28K bps. Memory IC and Audio circuits which include a microphone, speaker, amplifier etc., are externally connected to complete the voice recording and reproducing module. All Input pins are CMOS compatible. Typical applications Include voice storage, voice response, telecommunication and other voice fields.

### Pin Configuration




### Block Diagram



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### Absolute Maximum Ratings*

Supply Voltage, $V_{DD} - V_{SS}$ . . . . . 0 to 7V

Input Voltage, $V_{IN}$ . . . . . $V_{SS}$ to $V_{PD}$

Operating Temperature, $T_{OP}$ . . . . . −10°C to 60°C

Storage Temperature, $T_{ST}$ . . . . . −20°C to 80°C

### *Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### Electrical Characteristics

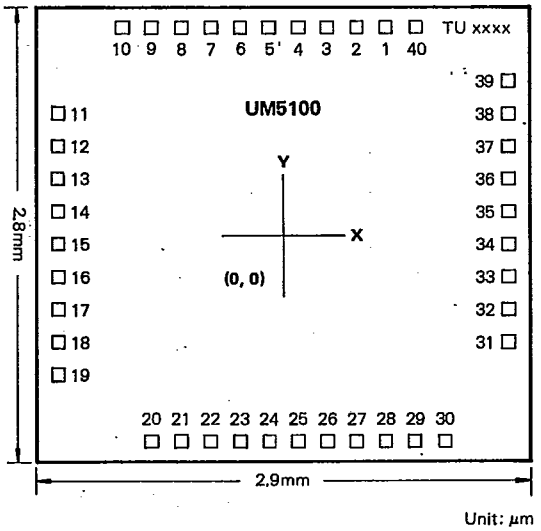
($V_{DD}$ = 5V, $F_{OSC}$ = 40 KHz, unless otherwise specified)

| Symbol | Parameter | | Limit | | | Units |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{DD}$ | Supply Voltage | | 3 | 5 | 6 | V |
| $I_{DD}$ | Stand-by Current | | | 1.0 | | μA |
| $I_{drive}$ | Clock Drive Current | | 16 | | | mA |
| $I_{sink}$ | Clock Sink Current | | 16 | | | mA |
| $V_{IH}$ | Input Voltage | High | 3.5 | | 5 | V |
| $V_{IL}$ | | Low | 0 | | 1.5 | V |
| $I_{drive}$ | *Output Current | Drive | 3 | 4 | | mA |
| $I_{sink}$ | | Sink | 3 | 4 | | mA |
| $T_{Reset}$ | Reset Pulse | | 1 | | | μS |
| $T_{Write}$ | Write Pulse Width | | 200 NS | | 10 μS | |

Note: *Except $A_0$, $D_6$ pin.

### Bonding Diagram

| Pad No. | X | Y | Pad No. | X | Y |
|---|---|---|---|---|---|
| 1 | 749 | 1208 | 21 | −730 | 1208 |
| 2 | 539 | 1208 | 22 | −520 | 1208 |
| 3 | 329 | 1208 | 23 | −310 | −1208 |
| 4 | 119 | 1208 | 24 | −100 | −1208 |
| 5 | −91 | 1208 | 25 | 110 | −1208 |
| 6 | −301 | 1208 | 26 | 319 | −1208 |
| 7 | −511 | 1208 | 27 | 529 | −1208 |
| 8 | −721 | 1208 | 28 | 740 | −1208 |
| 9 | −931 | 1208 | 29 | 950 | −1208 |
| 10 | −1140 | 1208 | 30 | 1161 | −1208 |
| 11 | −1264 | 697 | 31 | 1264 | −691 |
| 12 | −1264 | 486 | 32 | 1264 | −481 |
| 13 | −1264 | 277 | 33 | 1264 | −271 |
| 14 | −1264 | 67 | 34 | 1264 | −61 |
| 15 | −1264 | −143 | 35 | 1264 | 149 |
| 16 | −1264 | −354 | 36 | 1264 | 359 |
| 17 | −1264 | −564 | 37 | 1264 | 569 |
| 18 | −1264 | −774 | 38 | 1264 | 779 |
| 19 | −1264 | −984 | 39 | 1264 | 989 |
| 20 | −956 | 1216 | 40 | 949 | 1208 |




Unit: μm

## Pin Description

$V_{DD}$
Positive power supply +3 ~ +6V operation voltage.

$V_{SS}$
Circuit GND potential.

$A_0 \sim A_{14}$
Address bus.

$D_0 \sim D_7$
Data bus.

$\overline{\text{RECORD}}$
Input pin, active Low. Triggering this input pin the chip will go into "speech analysis" mode.

$\overline{\text{WRITE PULSE}}$
Output pin, active Low. This pin generates one pulse each time the clock count advances eight cycles. This pin is active only in the "speech analysis" mode.

$\overline{\text{READ}}$
Output pin, active Low. This pin provides an output control signal for external memory. This pin is active only in the "speech synthesis" mode.

$\overline{\text{PLAY}}$
Input pin, active low. Triggering this pin, the chip will go into "speech synthesis" mode.

RESET
Input pin, active high. When activated, all the internal counters are cleared and the chip is disabled.

ANG and $\overline{\text{ANG}}$
Analogue voice signal outputs with opposite phase.

FILTER
Output pin. Produces envelope waveform with external integrator circuit.

ENVELOPE
Input pin. Envelope signal will go into this pin to modulate voice amplitude.

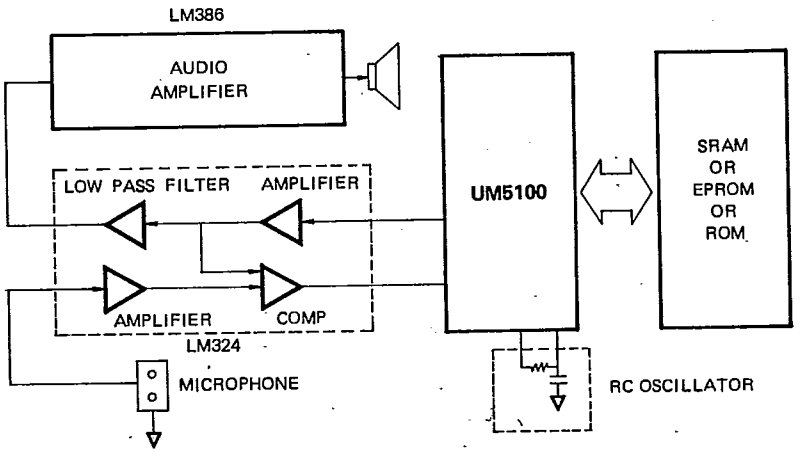
TD and $\overline{\text{TD}}$
Output pin. Auxiliary outputs for low frequency signal.

COMPDATA
Input pin. Detects the delta slope which is generated from the comparison of input signal and feedback signal.

C, R
RC oscillator pins, $f_{osc}$ = 40 KHz for R = 7.2K C = 0.0047μf

CLOCK DRIVER
Output pin for negative voltage generation.

## Talk Back Application Block Diagram




Voice Products

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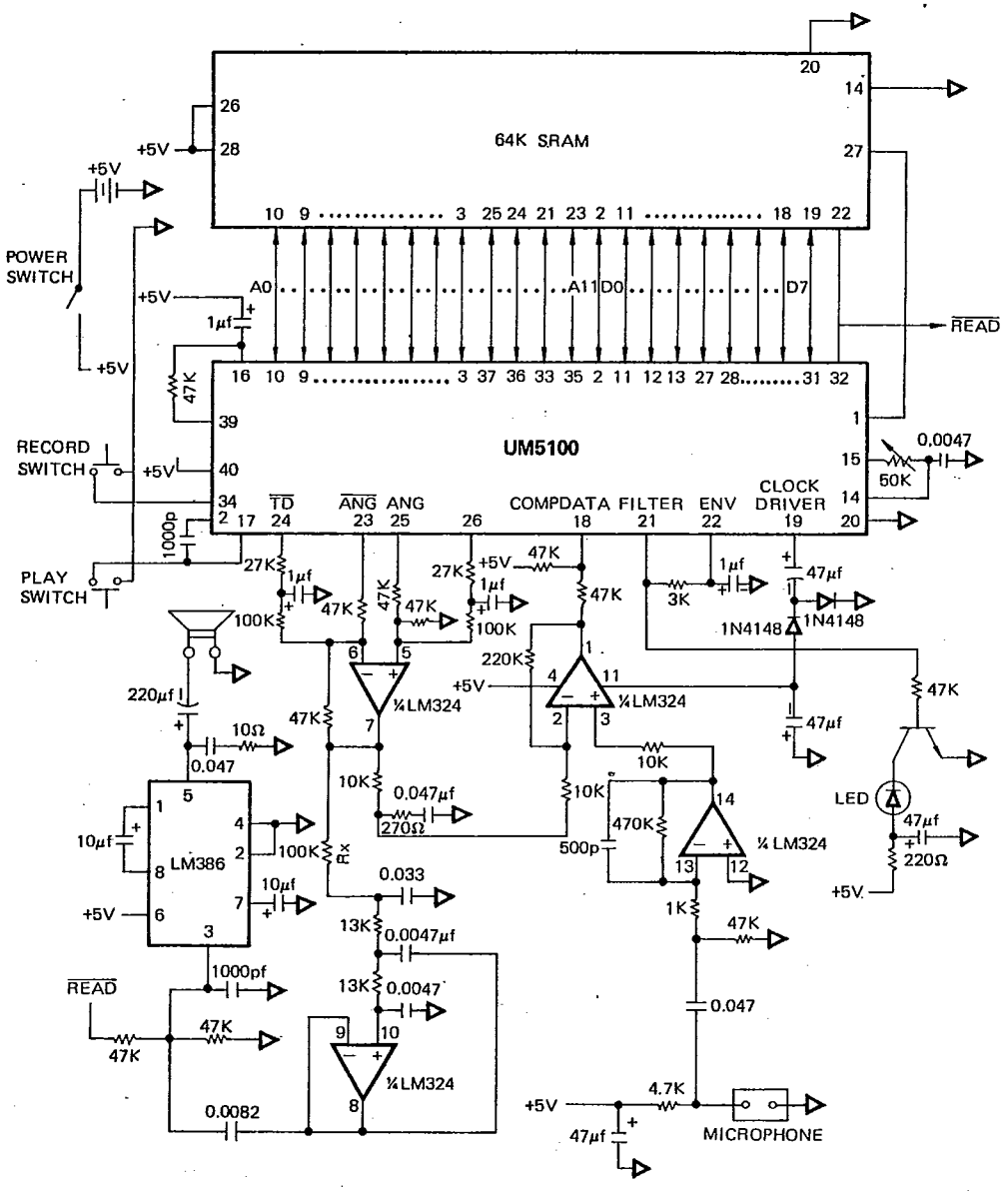
## SPEECH RECORDING AND PLAYBACK

(With power switch)



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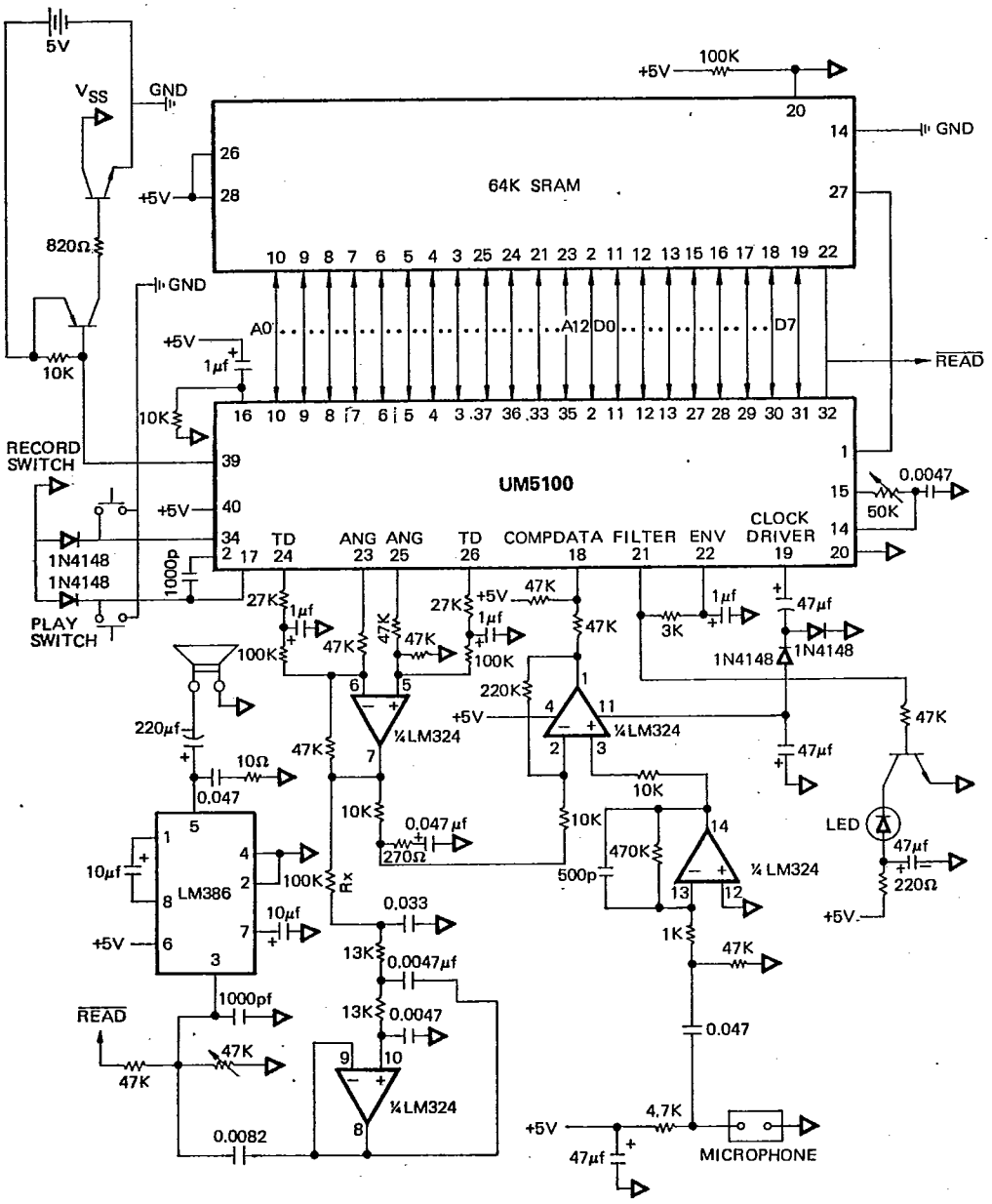
## Application Circuits

### SPEECH RECORDING AND PLAYBACK

(With low standby current)



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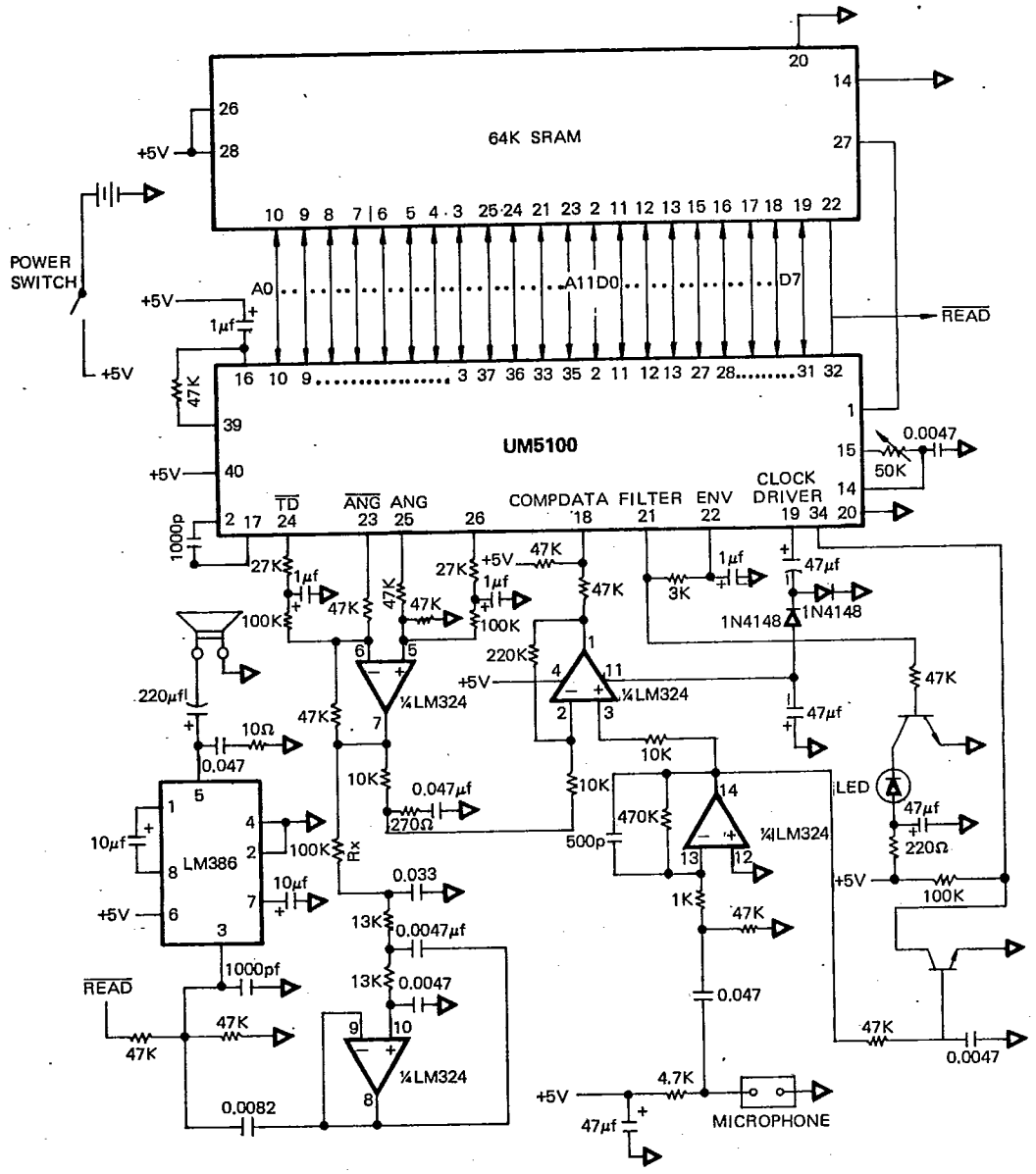
## SPEECH RECORDING AND PLAYBACK

(by voice trigger)



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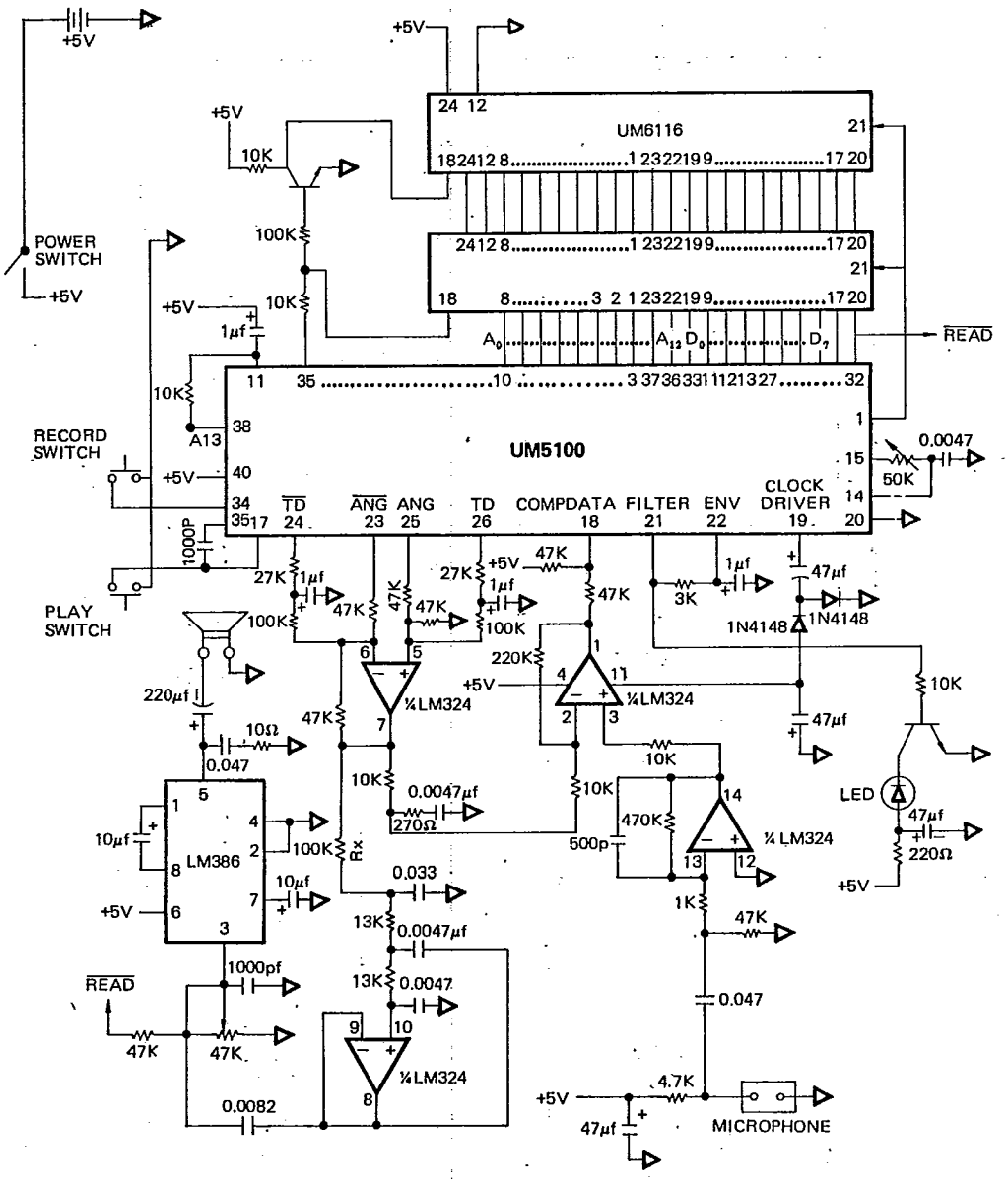
## SPEECH RECORDING AND PLAYBACK

(With 16K SRAM x 2)



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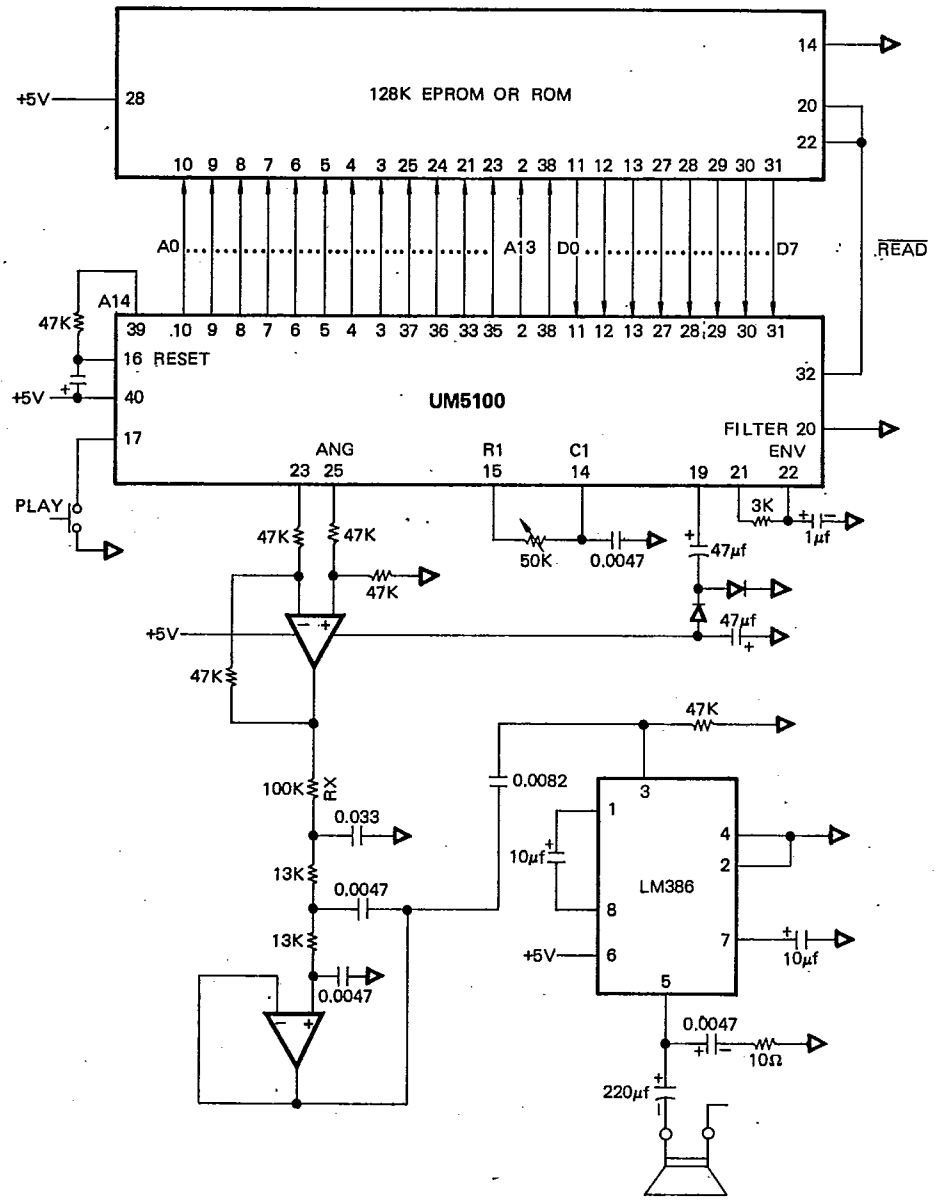
SPEECH SYNTHESIS